

## EE PART

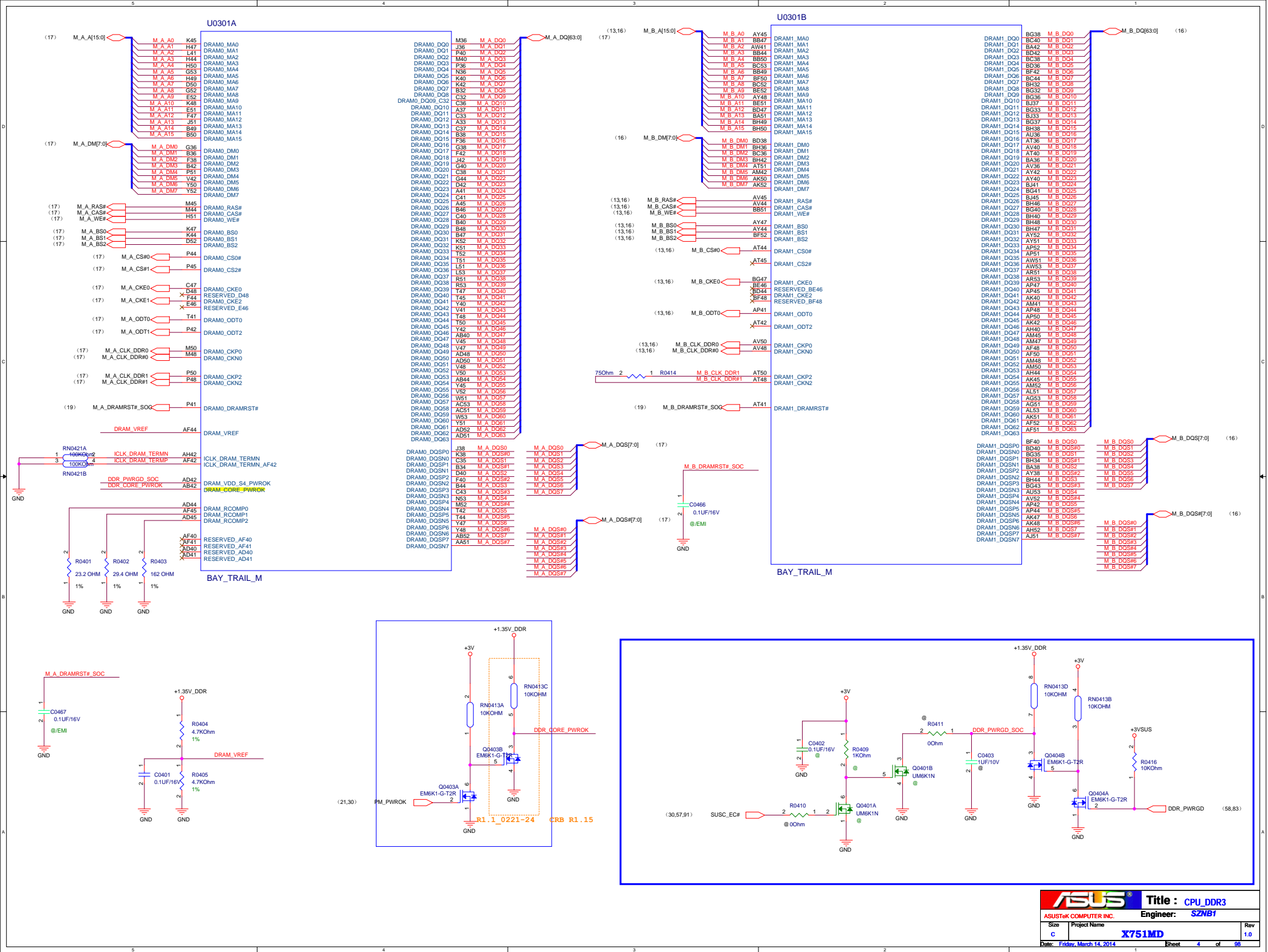
SKU Table

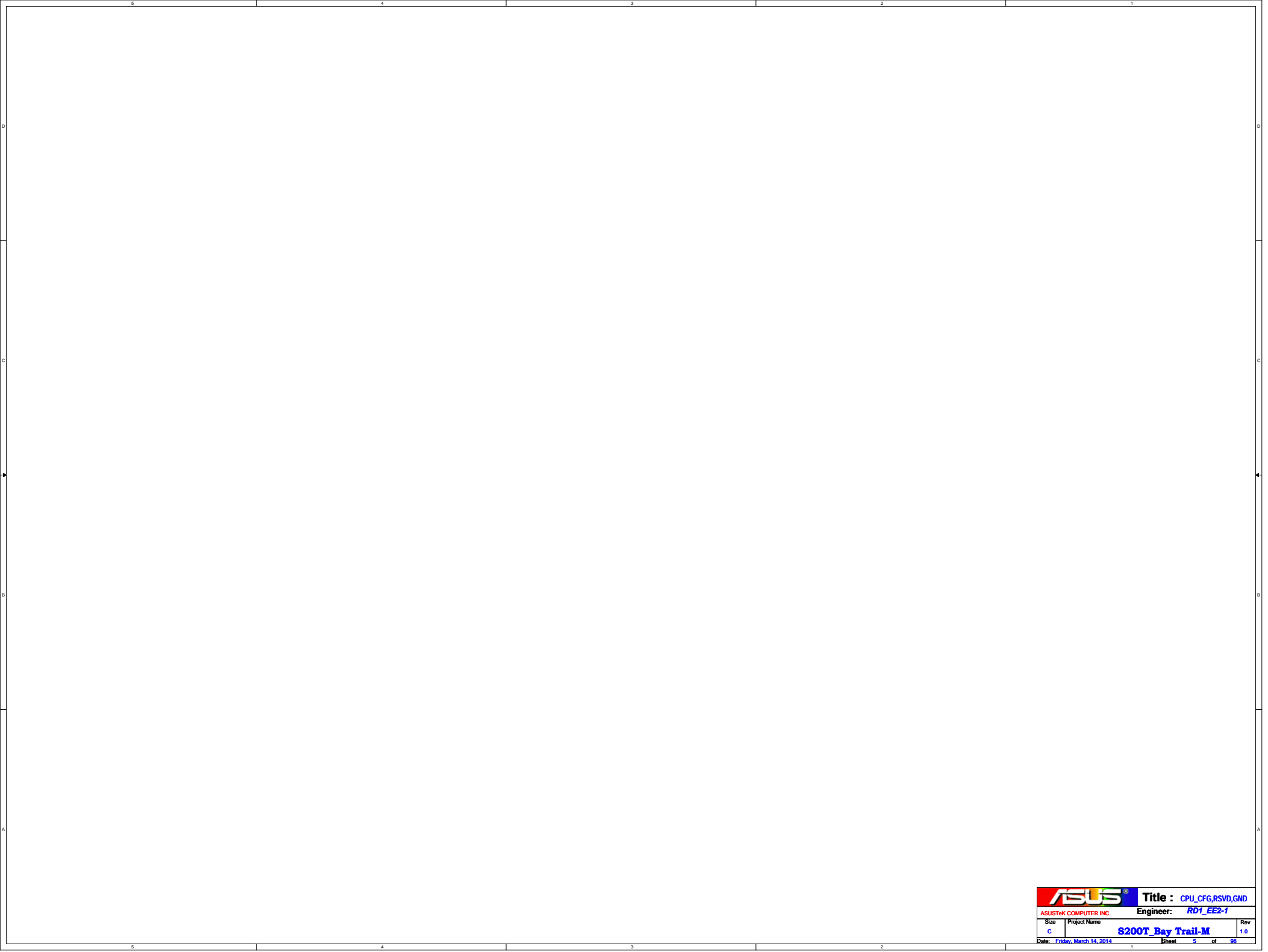
[illegible]





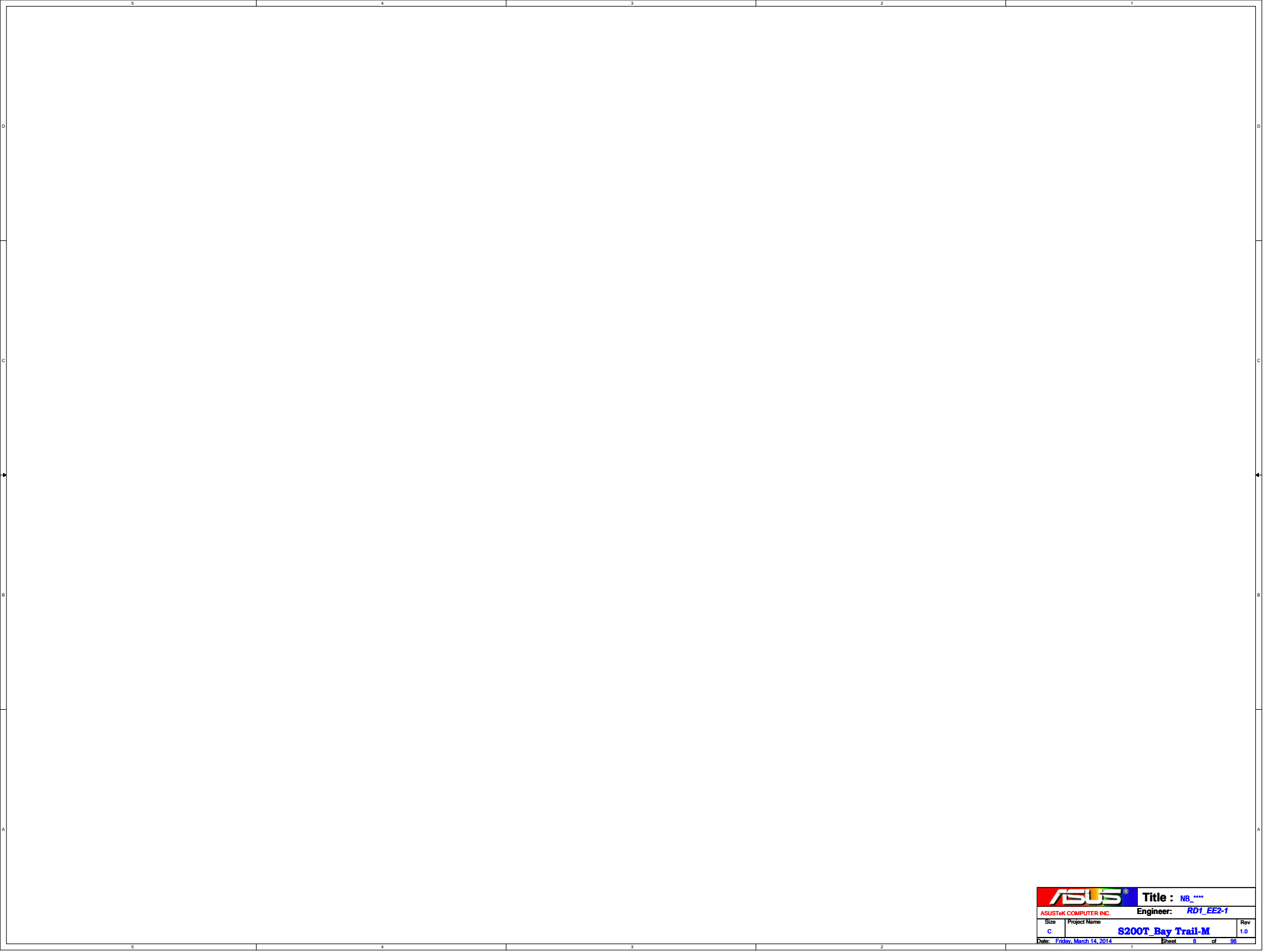


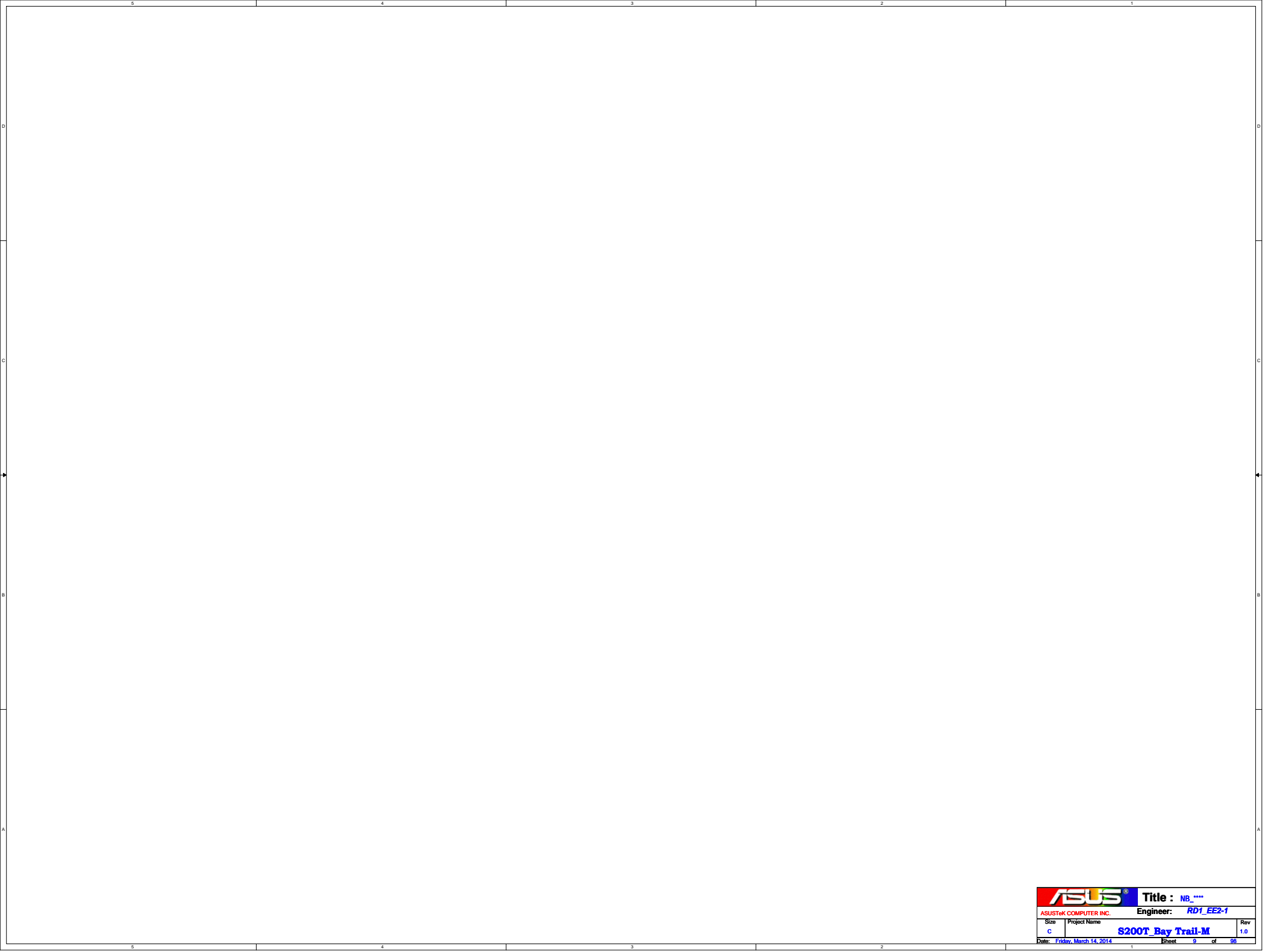


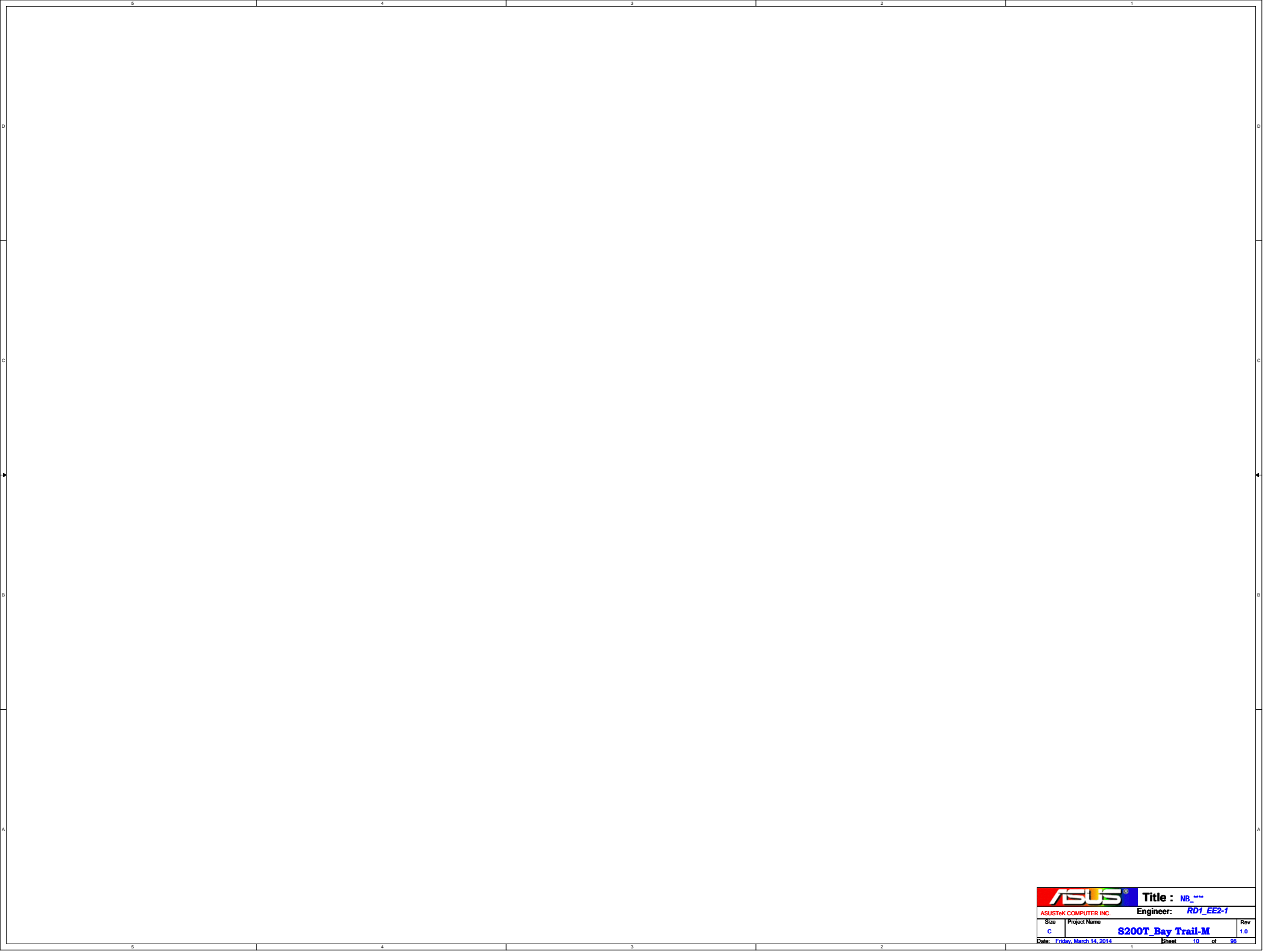


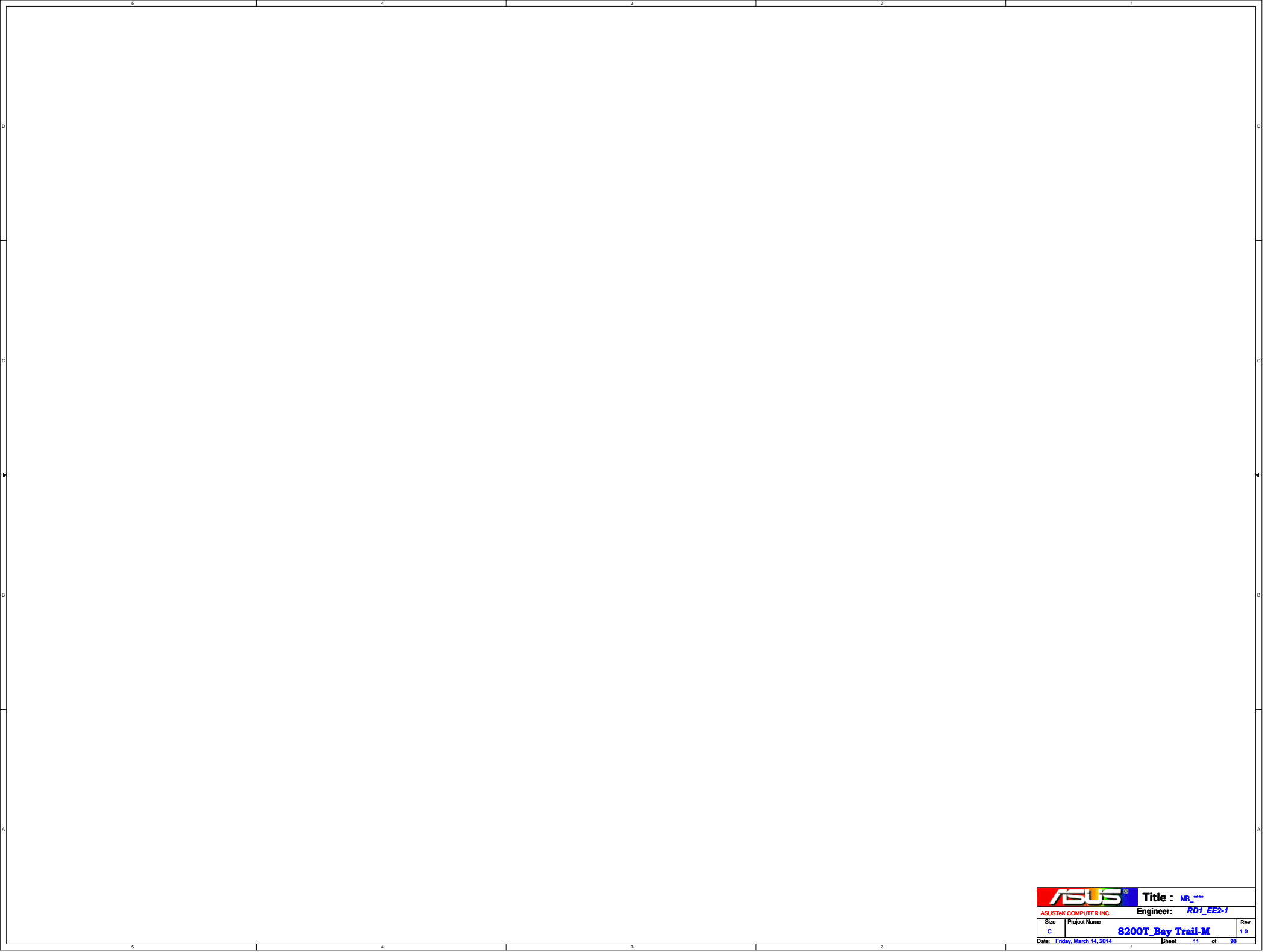




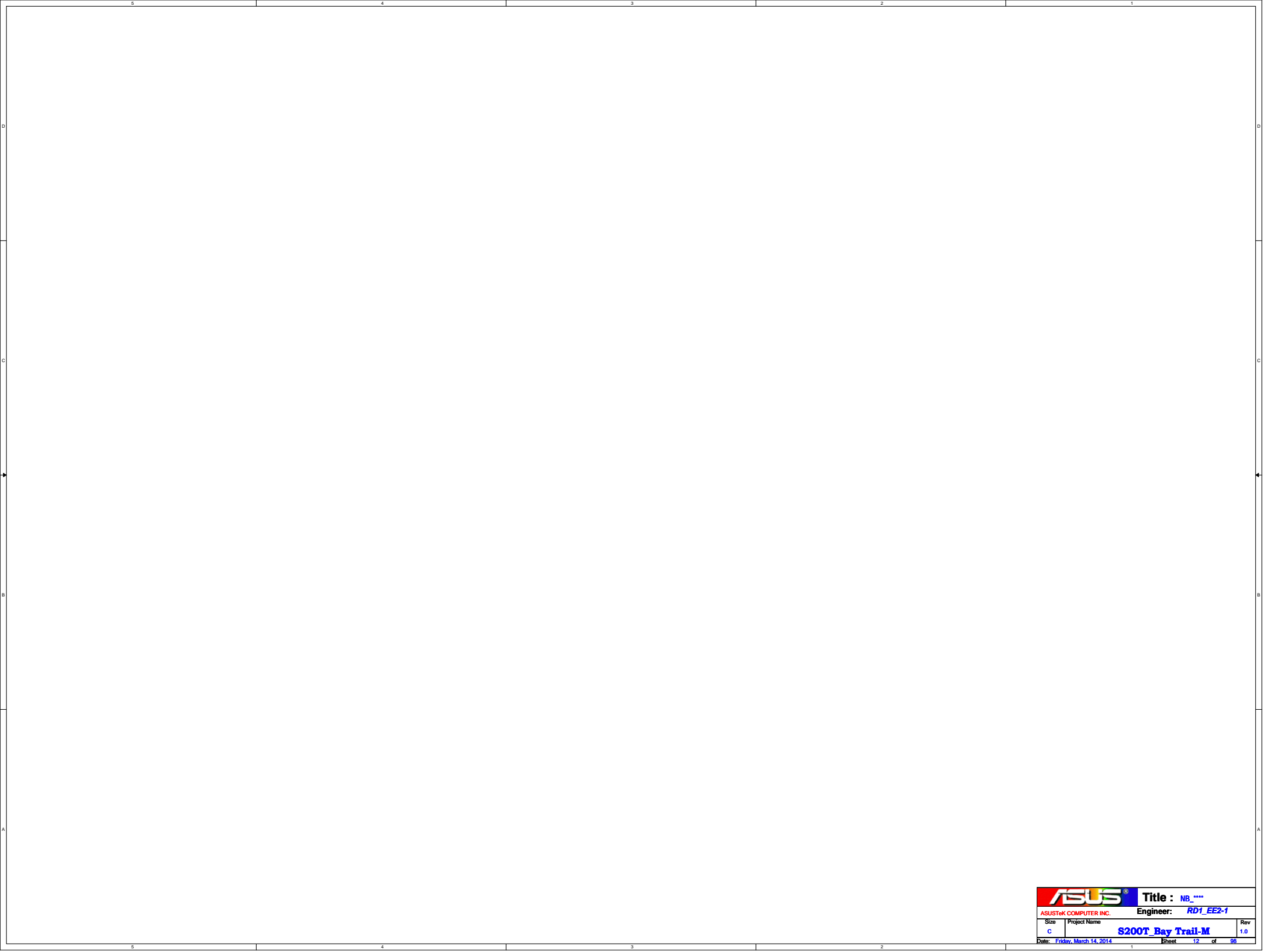




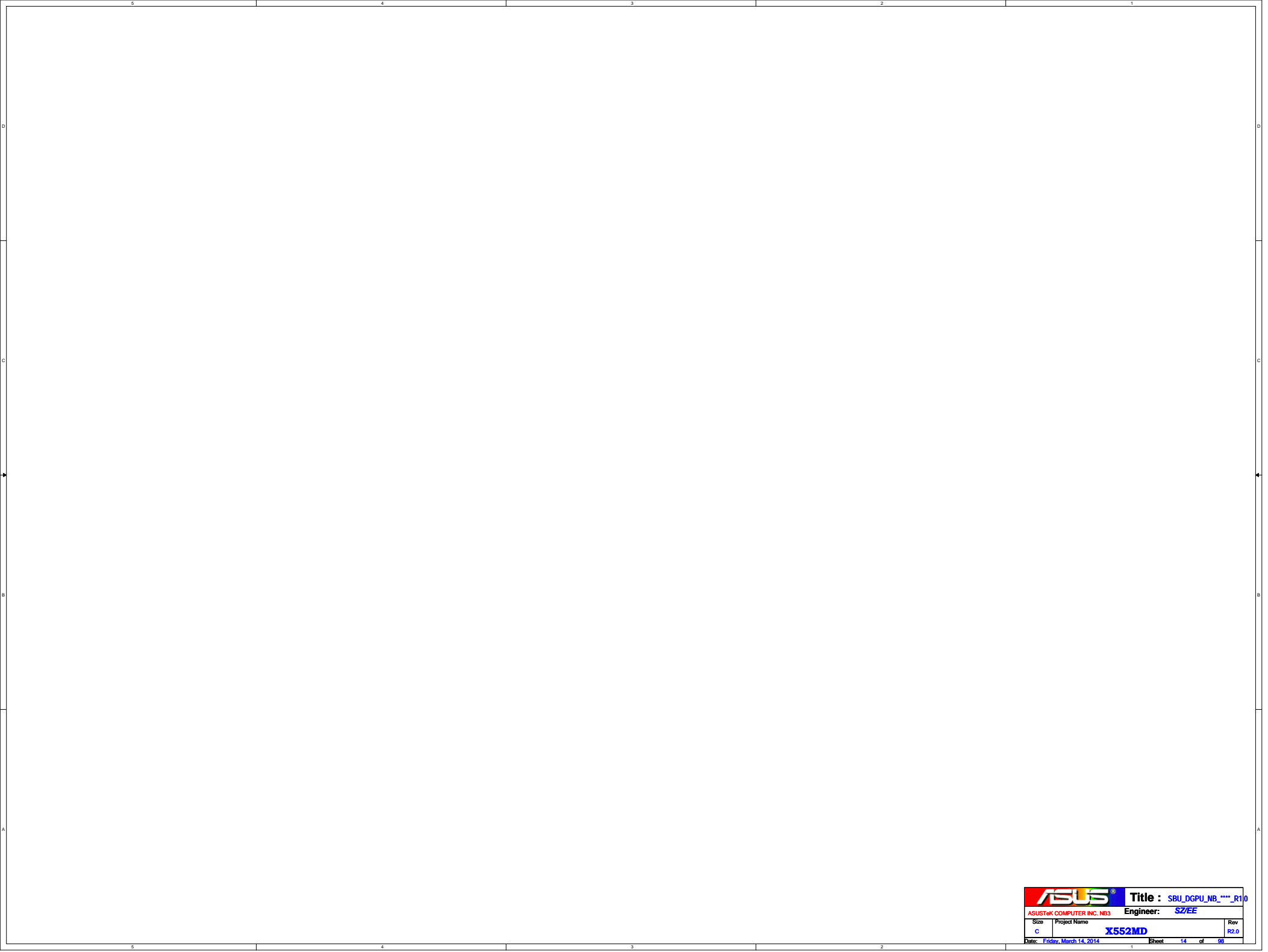


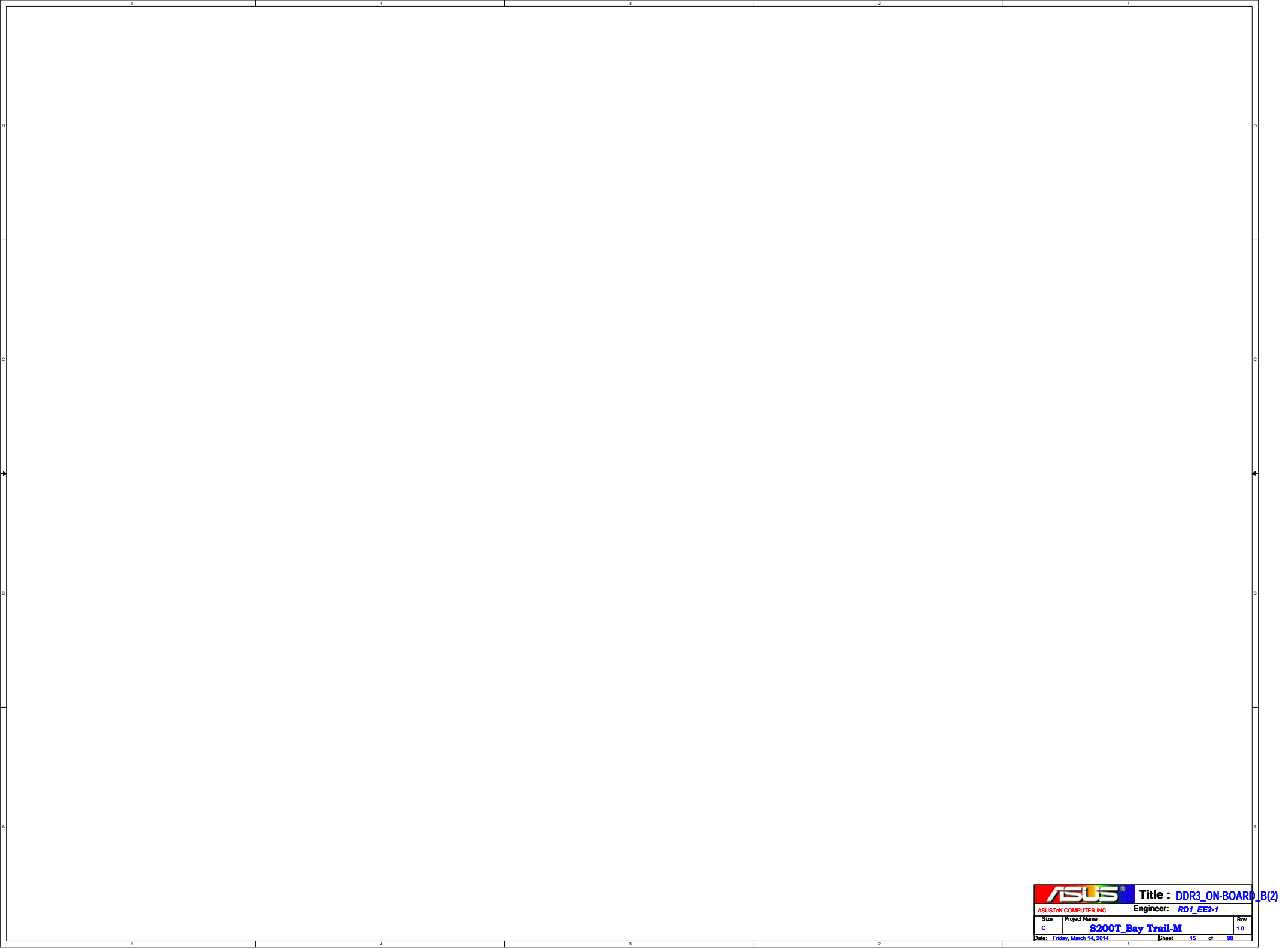


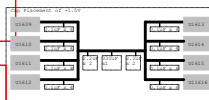




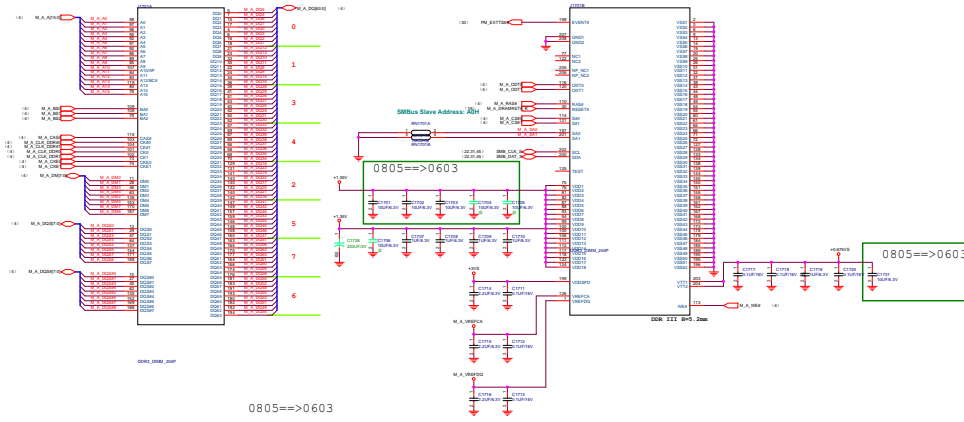


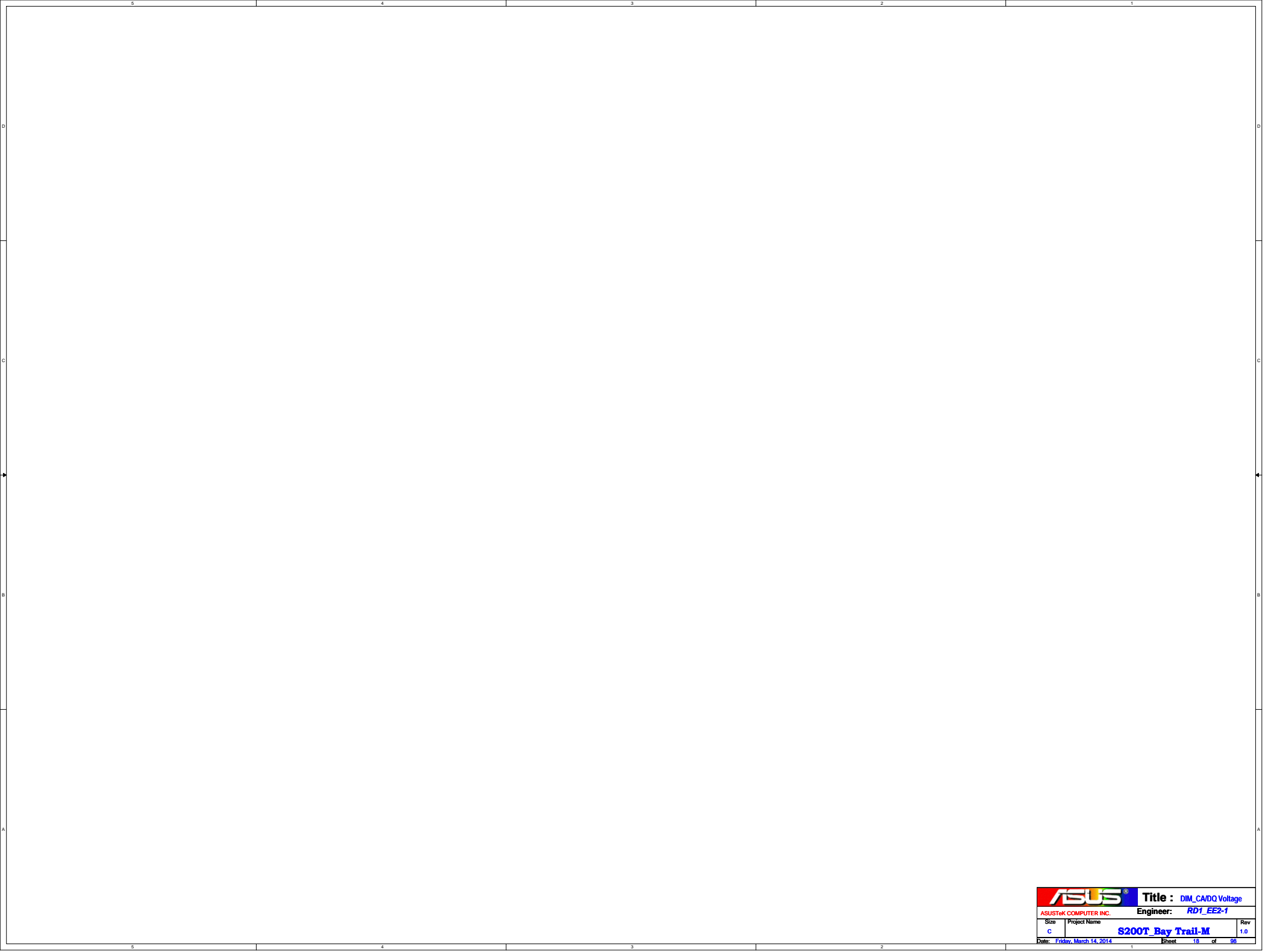






# SODIMM CHA-DIMM0

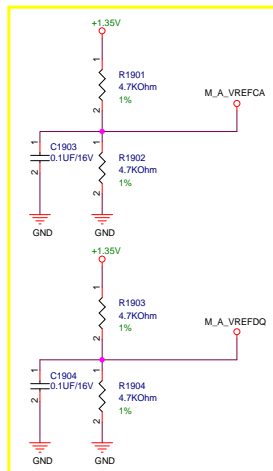
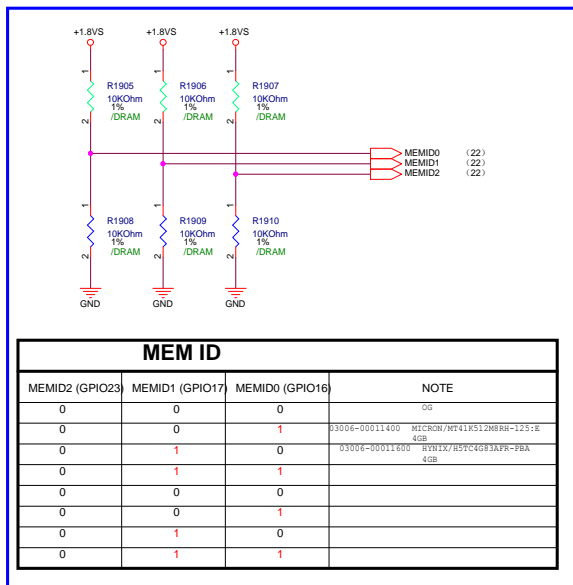




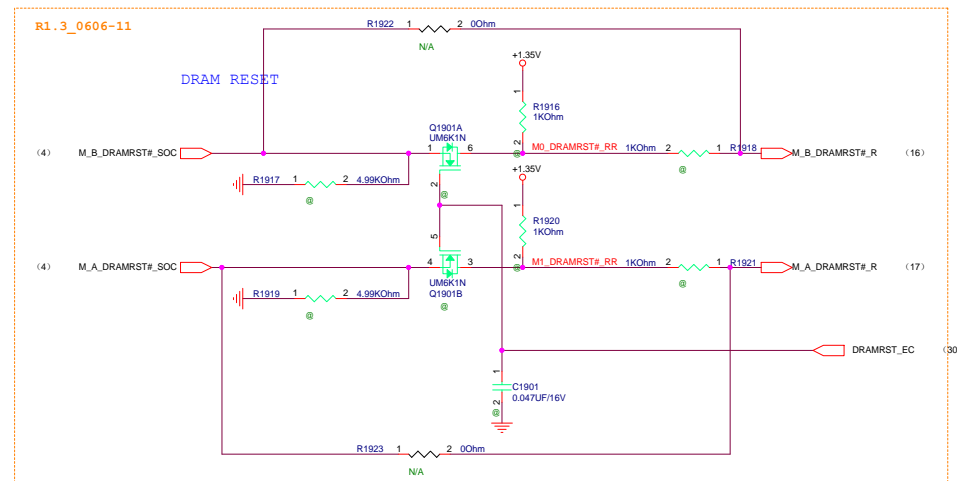
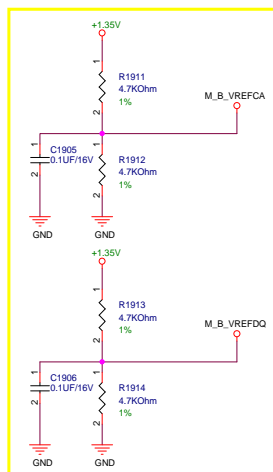
Calpella Clarksfield DDR3 SO-DIMM VREFDQ  
Platform Design Guide Change Details

## DDR3 Vref

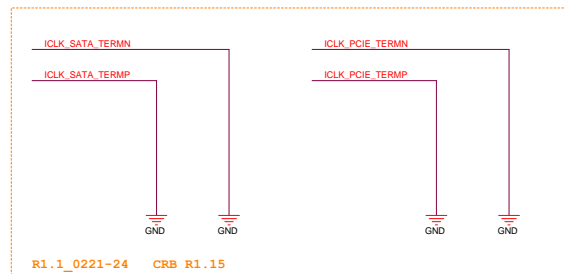
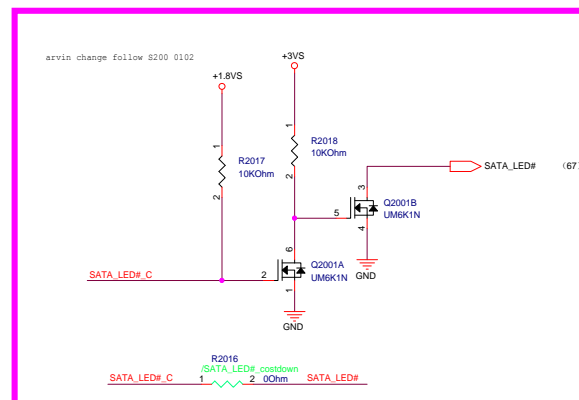
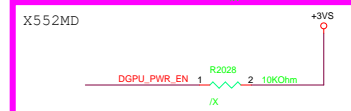
Intel Document Number: 400755



Near DIMM Device <5000 mil







## RTC Connector

BATT001

3V(220mAh)

07G016402032

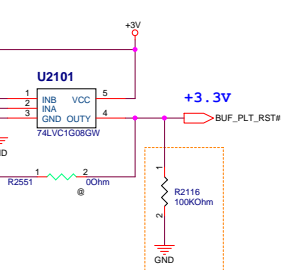
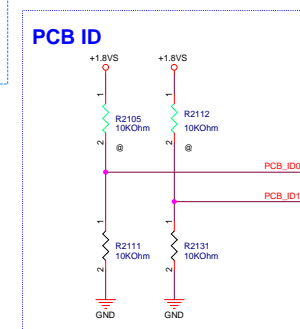
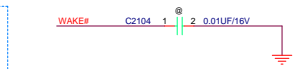
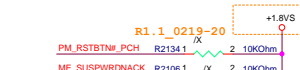
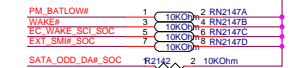
2nd source:

07G016B02032

07G016302032

07G0163L2032

For PU/PD



R1.1\_0208-12

ASUS

ASUSTeK COMPUTER INC. NBS

Size Custom

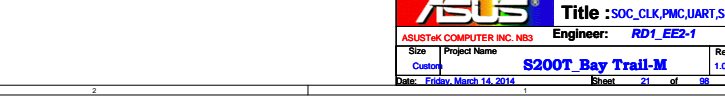
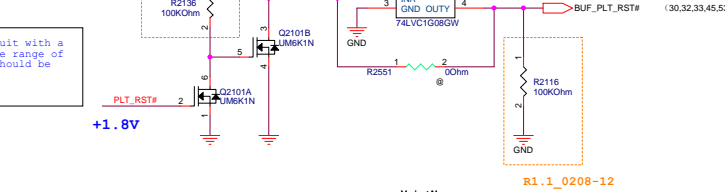
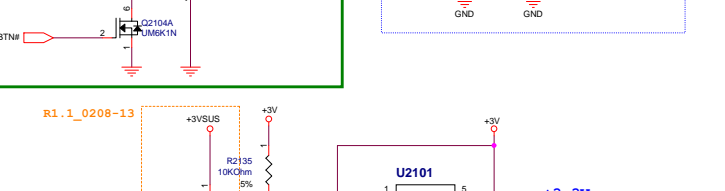
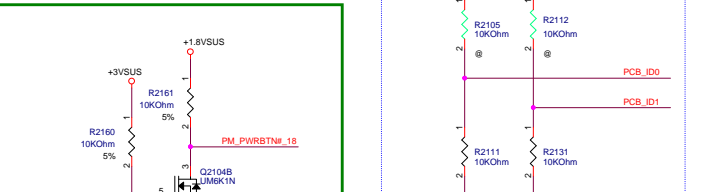
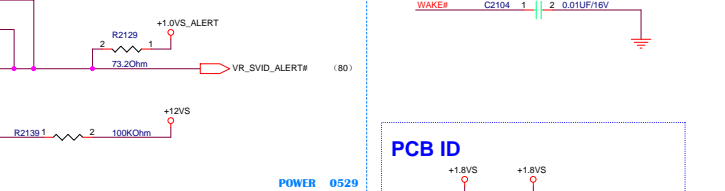
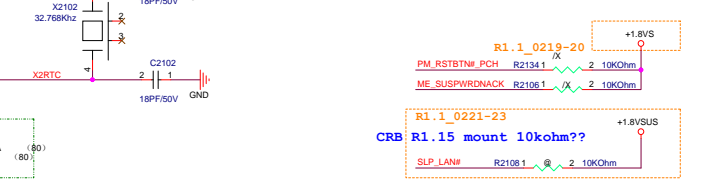
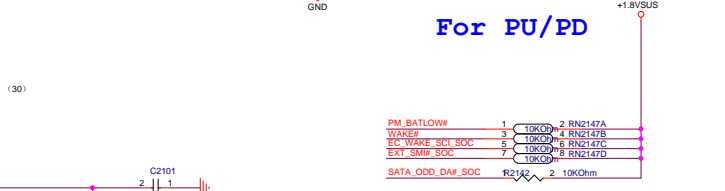
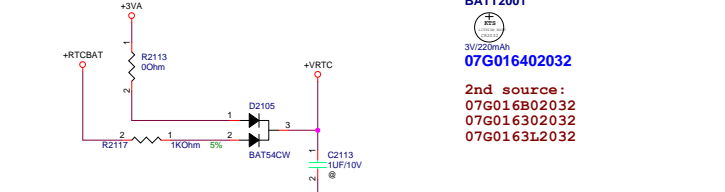
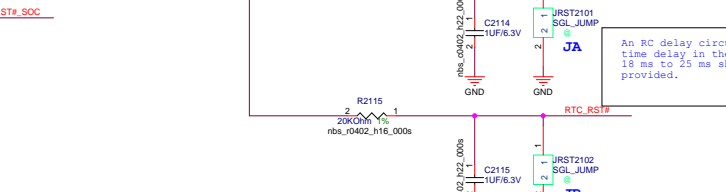
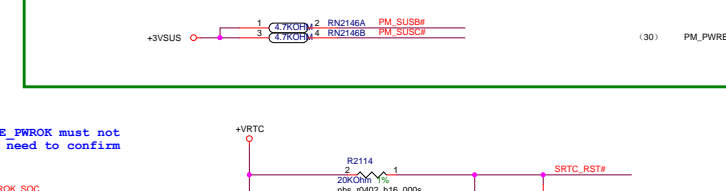
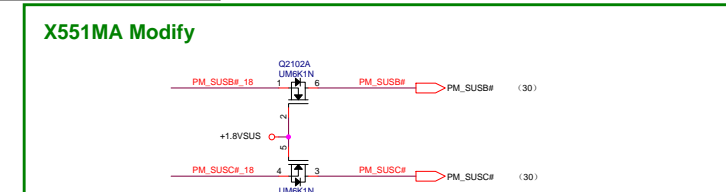
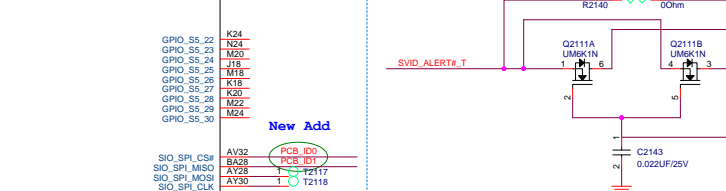
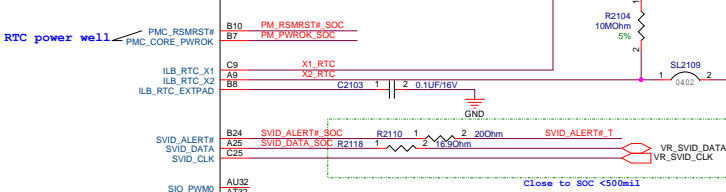
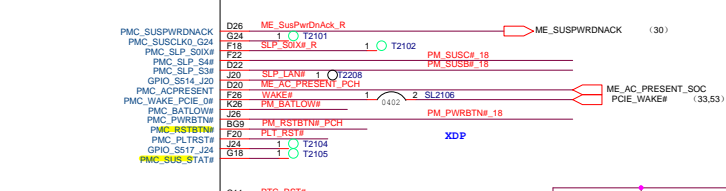
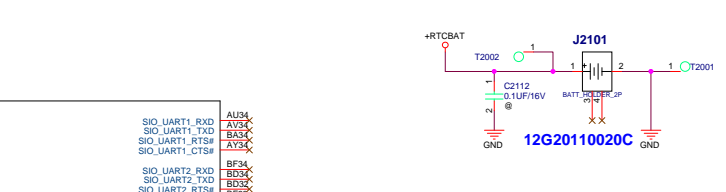
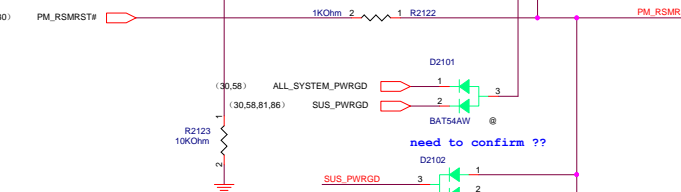
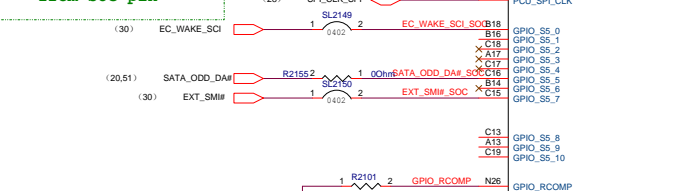
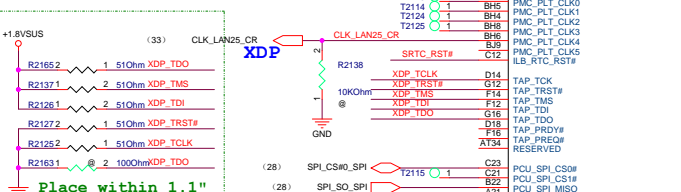
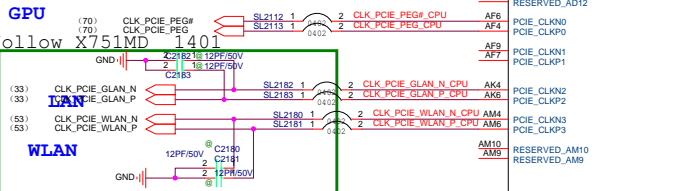
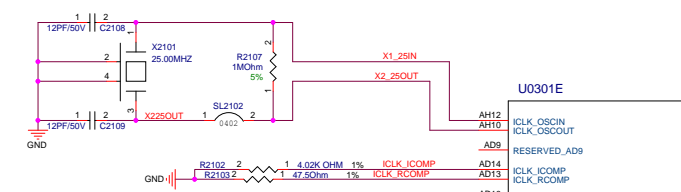
Project Name

Engineer: RD1\_EE2-1

Rev 1.0

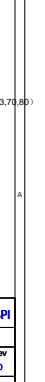
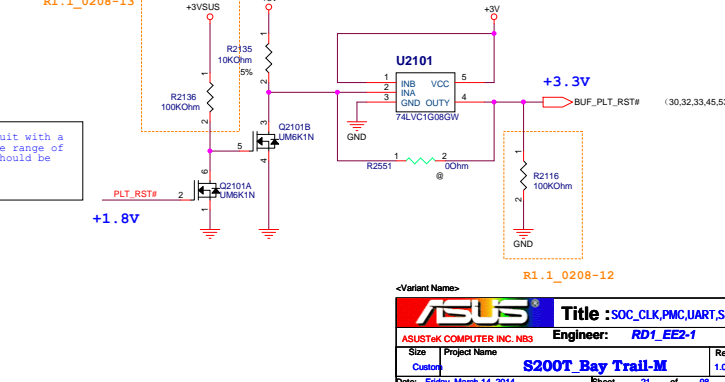
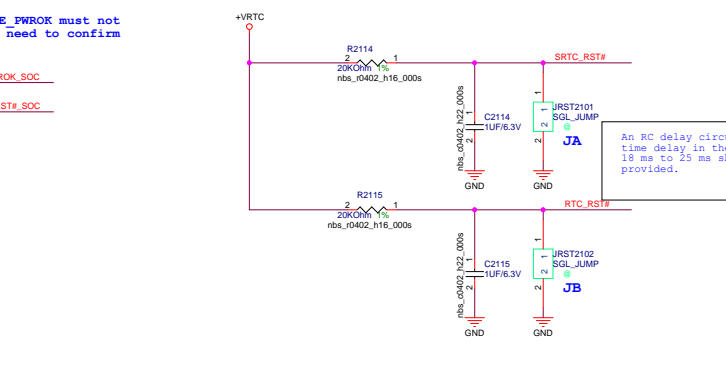
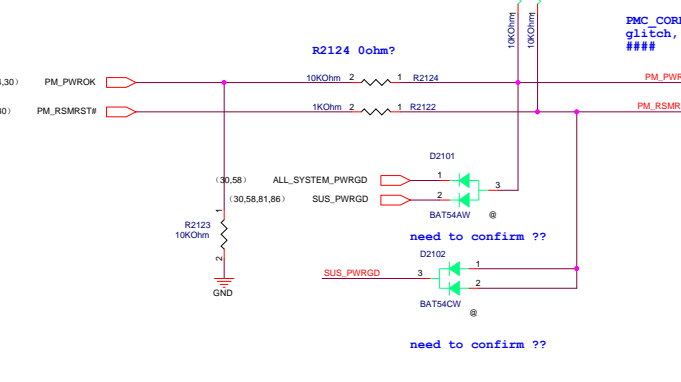
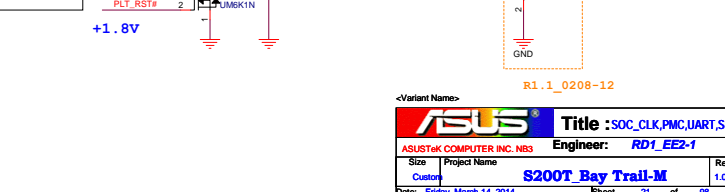
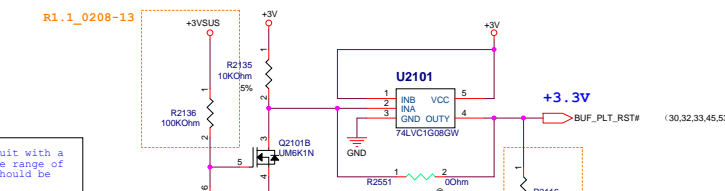
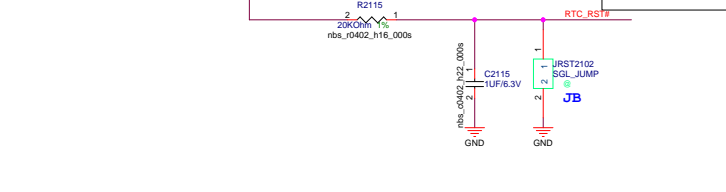
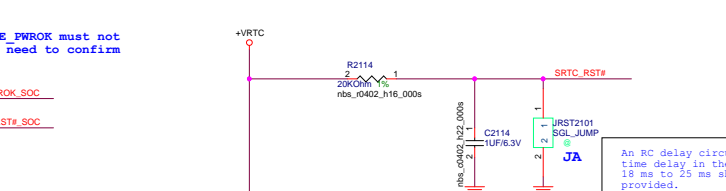
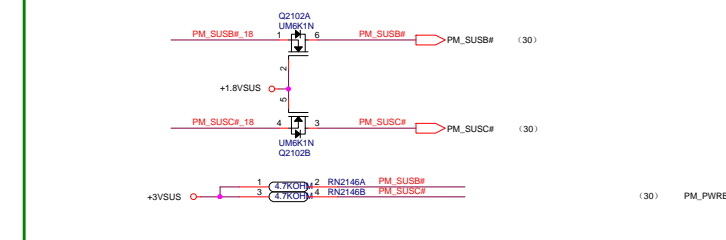
Date: Friday, March 14, 2014

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Power failure solution (S0-->G3, S5-->G3):


X551MA Modify







<Variant Name>



Title : CPU\_PCIE,USB

ASUSTeK COMPUTER INC. NB3

Engineer: RD1\_EE2-1


Size	Project Name	Rev
B	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014

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BOM



**Title :** CPU\_PCHCLOCK SIGNALS

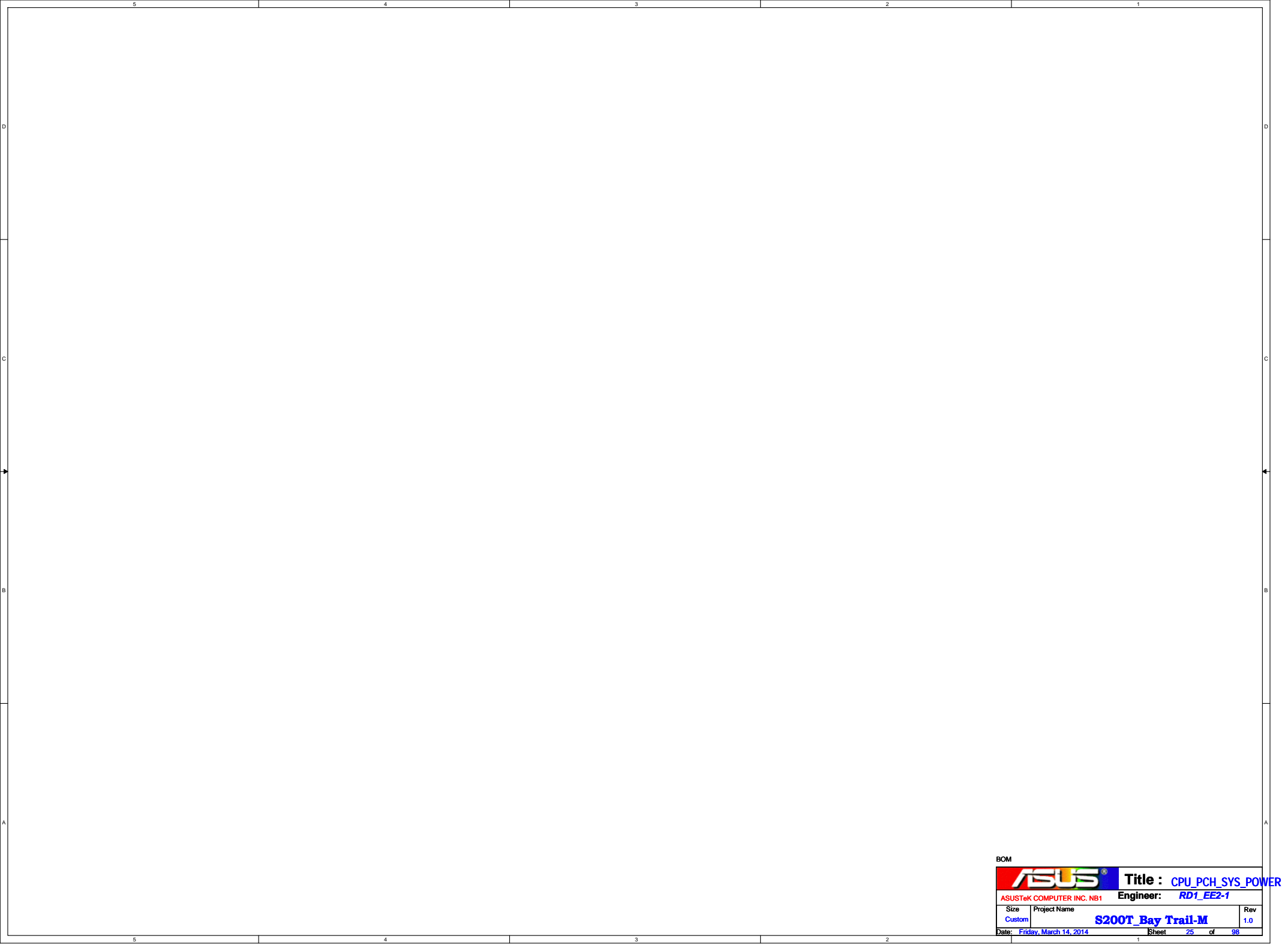
ASUSTeK COMPUTER INC. NB1

**Engineer:** RD1\_EE2-1


Size	Project Name	Rev
B	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014

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BOM



ASUSTeK COMPUTER INC. NB1

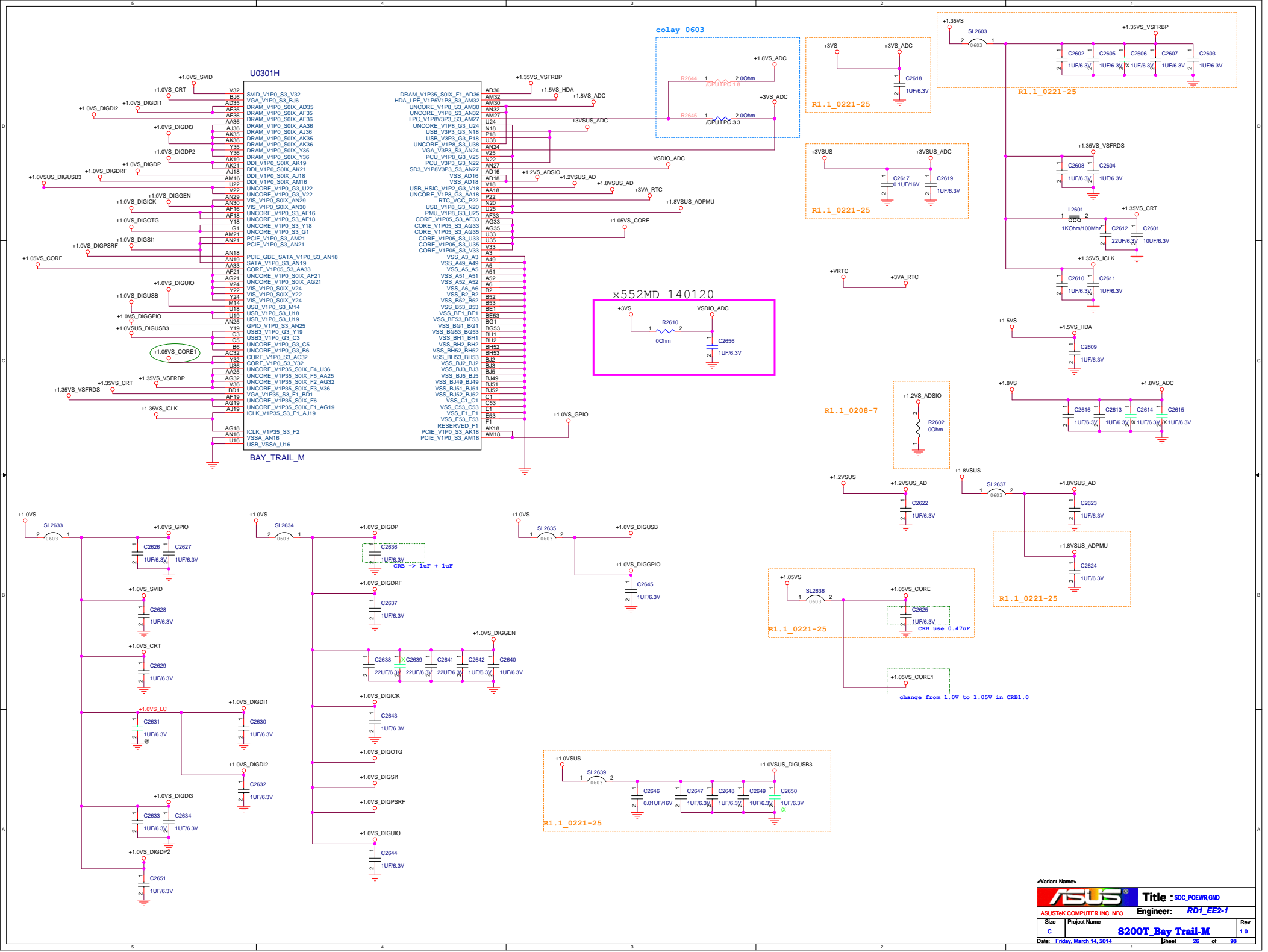
Size	Project Name	Rev
Custom	S200T Bay Trail-M	1.0

Title : CPU\_PCH\_SYS\_POWER

Engineer: RD1\_EE2-1

Date: Friday, March 14, 2014

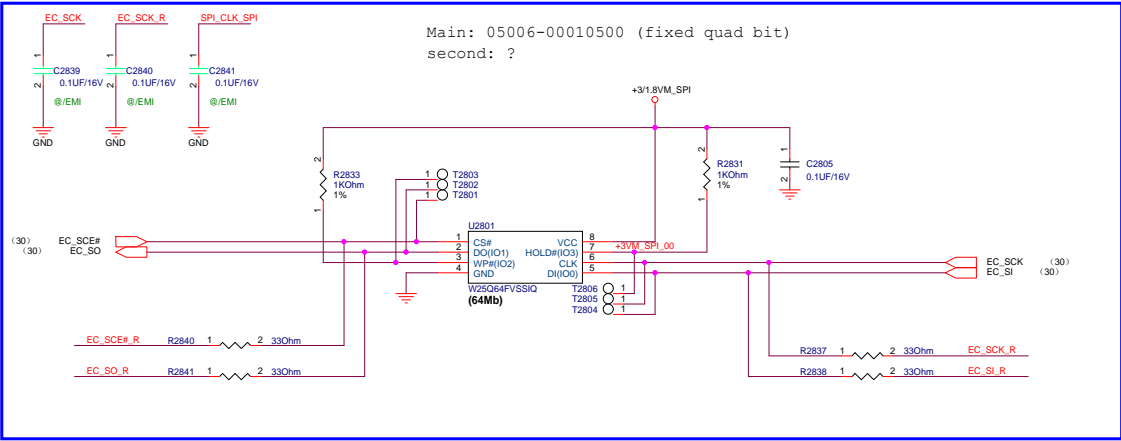
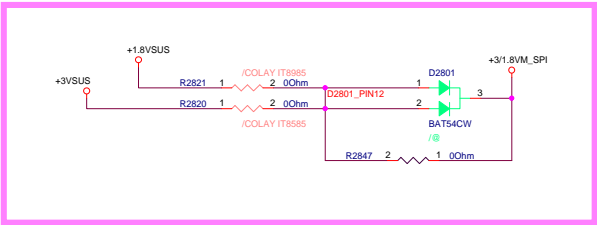
Sheet 25 of 98





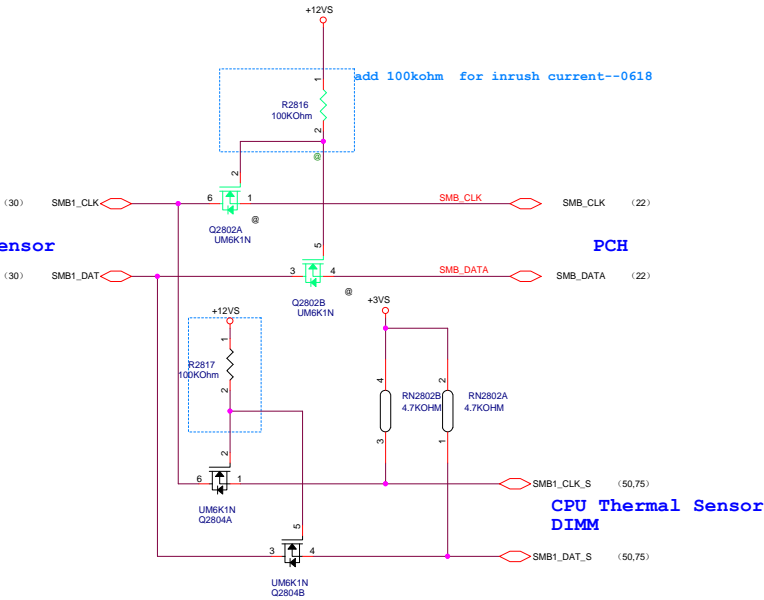


PCH SPI ROM



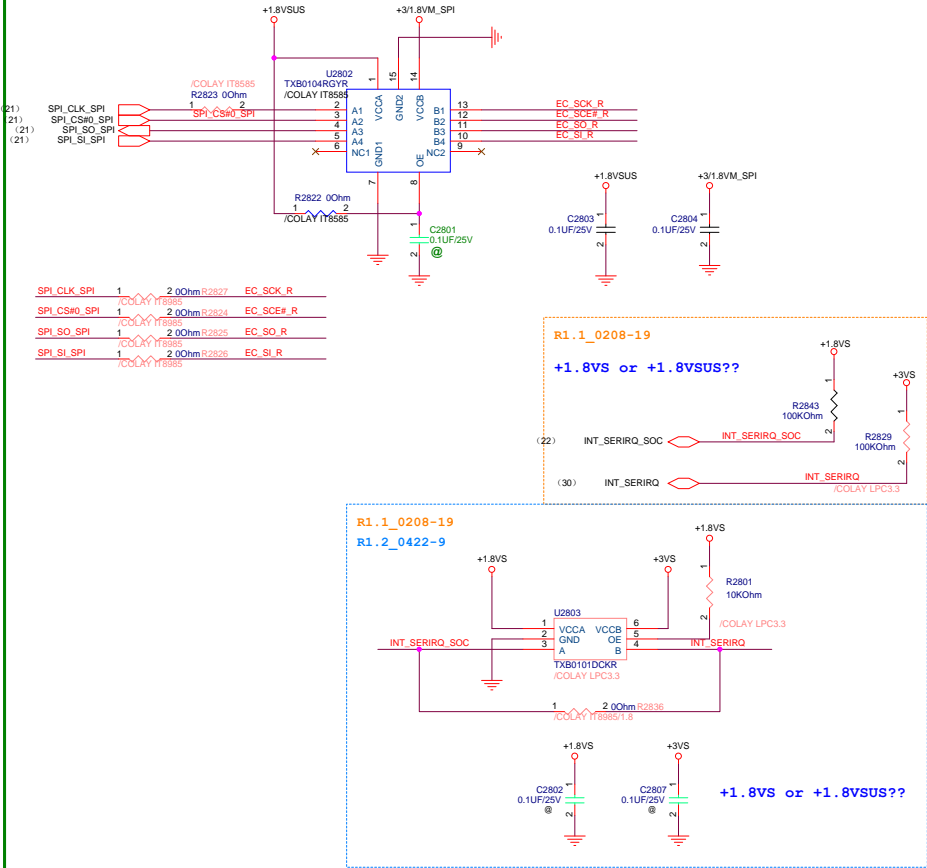
SMBus

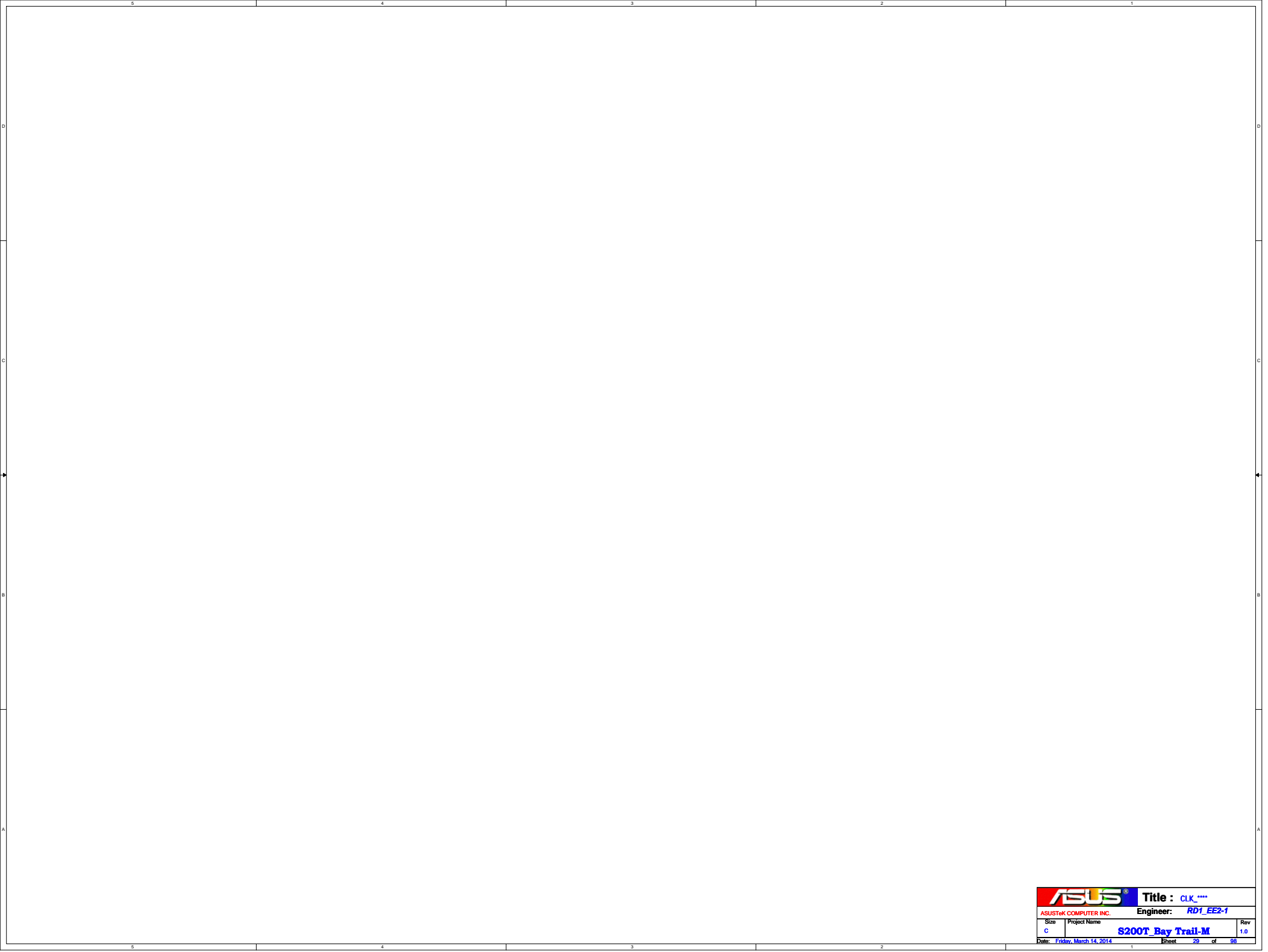
EC  
CPU/ GPU Thermal Sensor



X551 Modify refer to X102MA

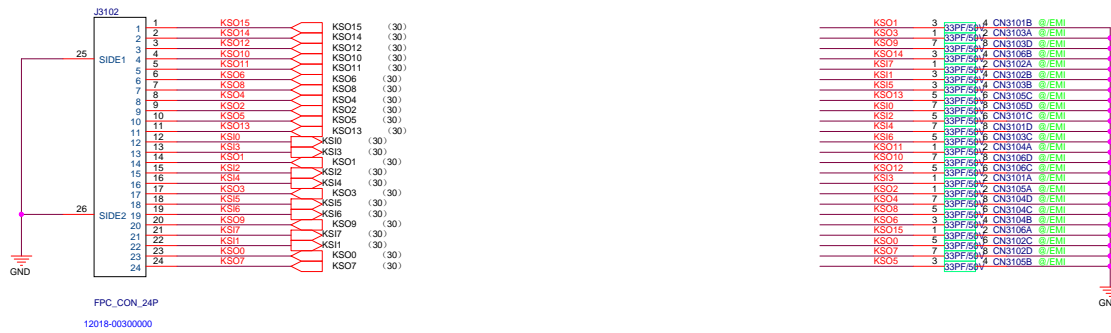
+1.8VS or +1.8VSUS??



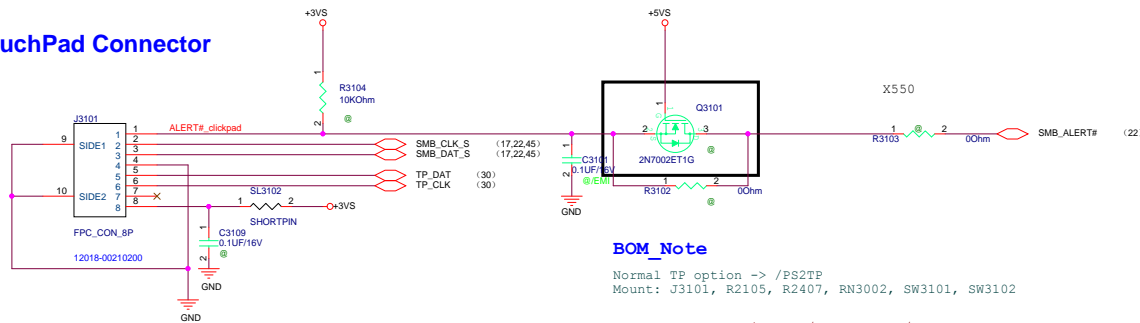




## Keyboard Connector



## TouchPad Connector



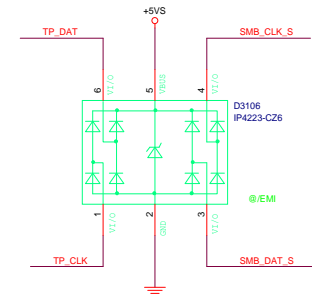
## BOM\_Note

Normal TP option -> /PS2TP  
Mount: J3101, R2105, R2407, RN3002, SW3101, SW3102

ELAN SMBUS TP option -> /ELAN\_PAD + /CPAD  
Mount: R2106, R2408, RN3008, Q3102, J3104

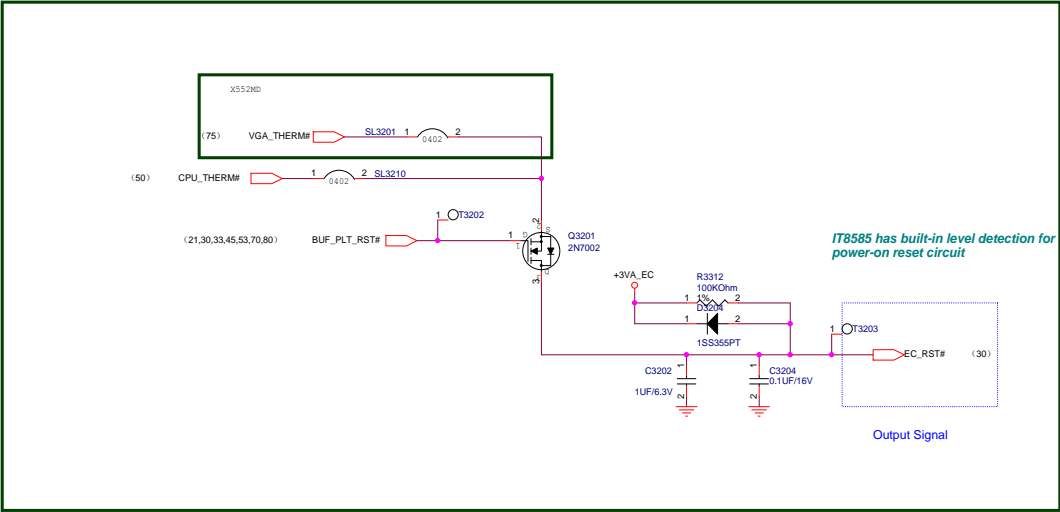
Synaptics SMBUS TP option -> /CPAD  
Mount: J3104, R2408, RN3008

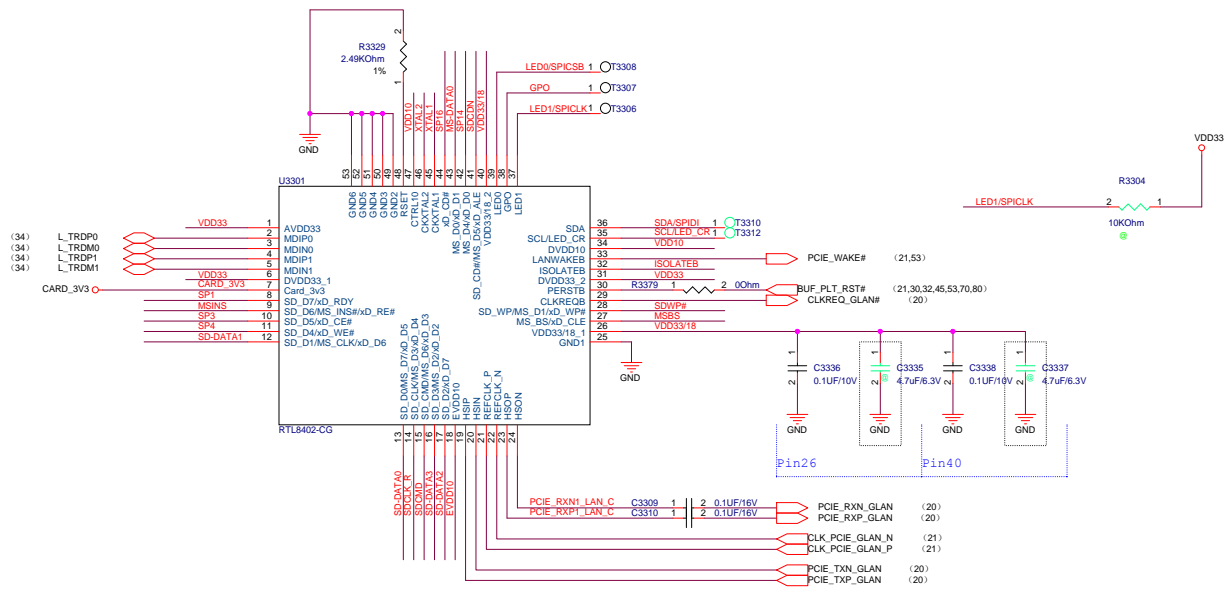
## Reserved for EMI



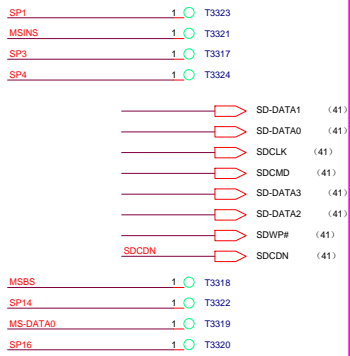
&lt;Variant Name&gt;

Thermal Policy

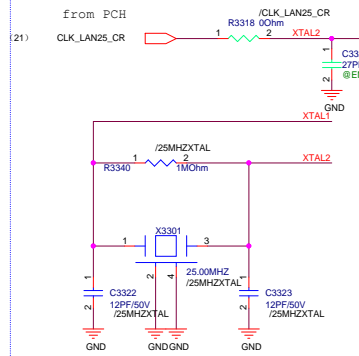




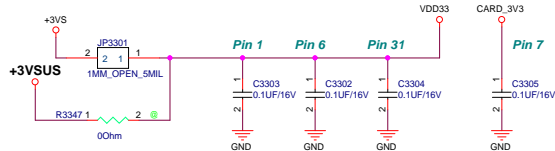
### Card Reader Interface



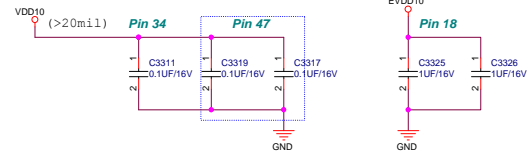
### arvin change 140115

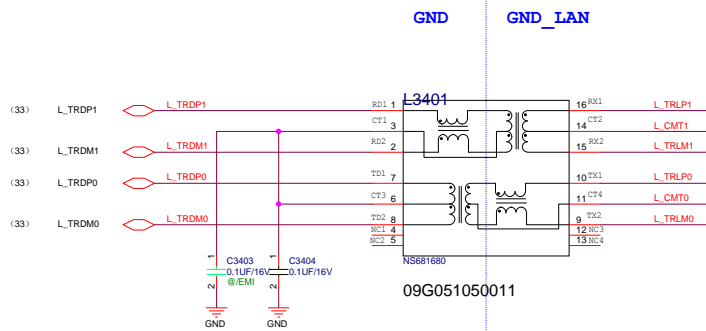
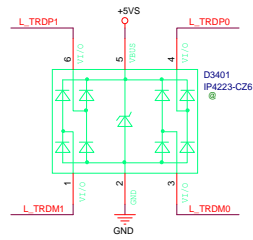


### 3.3V POWER

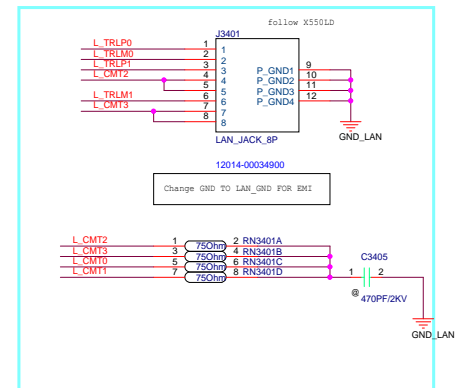
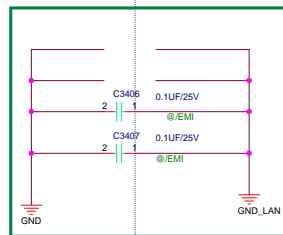


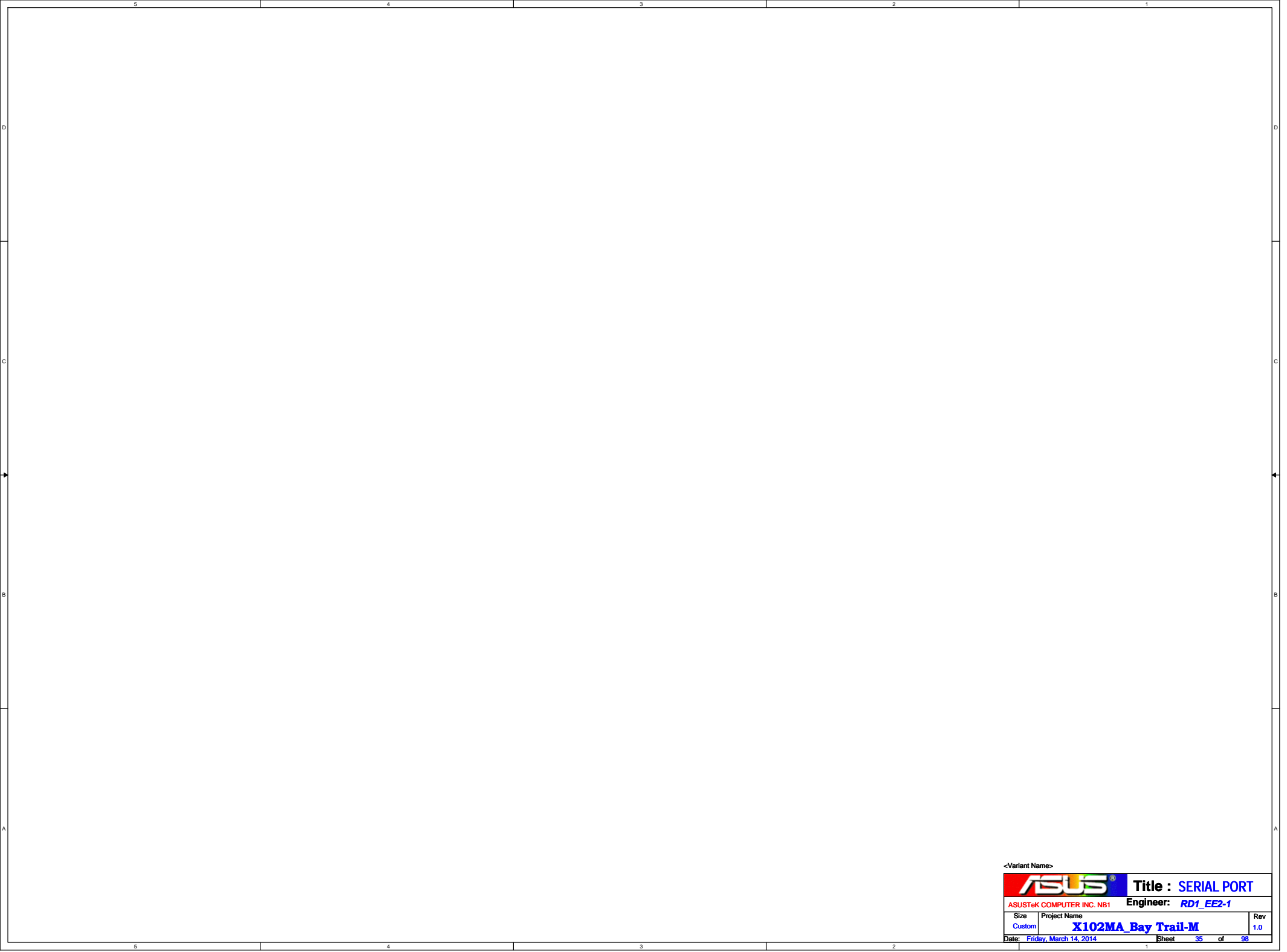
### 1V POWER



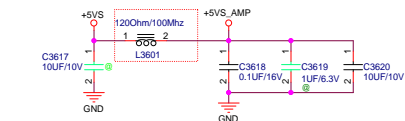


C3403,C3404 close to L3401 pin3 and pin6 each

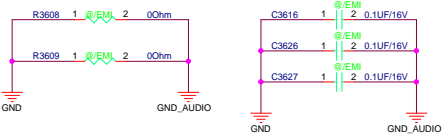
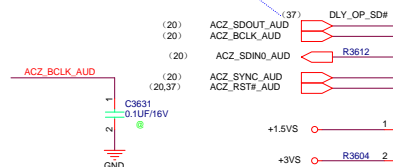








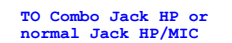
**Class D power down control pin**  
0:Power Down;1:Power Up



The schematic diagram illustrates the ANALOG section of a circuit, centered around the U3601 ADC. Key components and connections include:

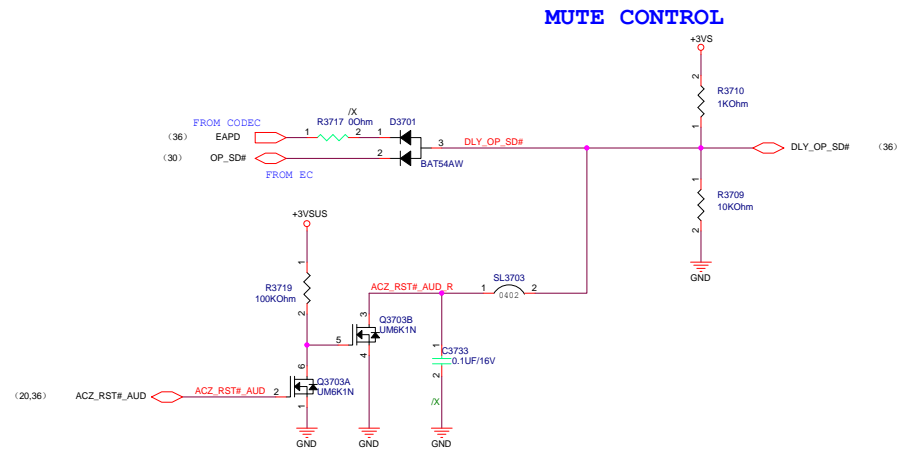
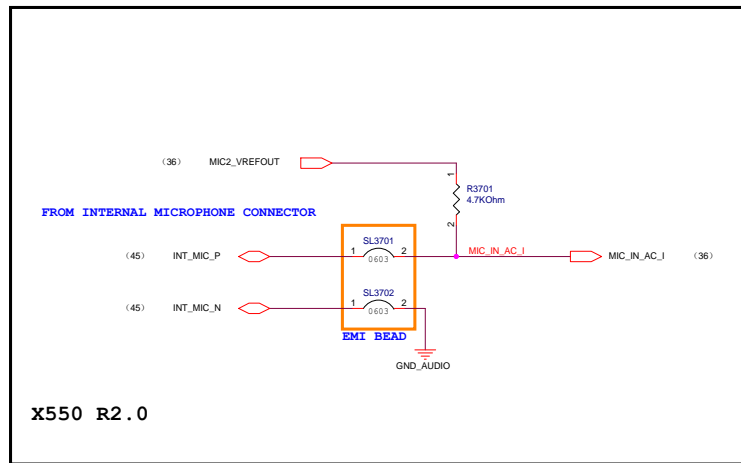
- U3601 ADC:** The central component with pins for digital control (D1-D4, PDI, BCLK, DVS, SDATA-IN, SYNC, RESET#, PCBEEP), analog inputs (SPKIN+, SPKIN-, SPKOUT+, SPKOUT-), and power/ground connections (GND1, GND2, PVD2, PVD3, PVD4, PVD5, PVD6, PVD7, PVD8, PVD9, PVD10, PVD11, PVD12, PVD13, PVD14, PVD15, PVD16, PVD17, PVD18, PVD19, PVD20, PVD21, PVD22, PVD23, PVD24, PVD25, PVD26, PVD27, PVD28, PVD29, PVD30, PVD31, PVD32, PVD33, PVD34, PVD35, PVD36, PVD37, PVD38, PVD39, PVD40, PVD41, PVD42, PVD43, PVD44, PVD45, PVD46, PVD47, PVD48, PVD49, PVD50, PVD51, PVD52, PVD53, PVD54, PVD55, PVD56, PVD57, PVD58, PVD59, PVD60, PVD61, PVD62, PVD63, PVD64, PVD65, PVD66, PVD67, PVD68, PVD69, PVD70, PVD71, PVD72, PVD73, PVD74, PVD75, PVD76, PVD77, PVD78, PVD79, PVD80, PVD81, PVD82, PVD83, PVD84, PVD85, PVD86, PVD87, PVD88, PVD89, PVD90, PVD91, PVD92, PVD93, PVD94, PVD95, PVD96, PVD97, PVD98, PVD99, PVD100).
- Power and Ground:** Connections for +5VS\_AUDIO, GND\_AUDIO, and various ground points (GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, GND9, GND10, GND11, GND12, GND13, GND14, GND15, GND16, GND17, GND18, GND19, GND20, GND21, GND22, GND23, GND24, GND25, GND26, GND27, GND28, GND29, GND30, GND31, GND32, GND33, GND34, GND35, GND36, GND37, GND38, GND39, GND40, GND41, GND42, GND43, GND44, GND45, GND46, GND47, GND48, GND49, GND50, GND51, GND52, GND53, GND54, GND55, GND56, GND57, GND58, GND59, GND60, GND61, GND62, GND63, GND64, GND65, GND66, GND67, GND68, GND69, GND70, GND71, GND72, GND73, GND74, GND75, GND76, GND77, GND78, GND79, GND80, GND81, GND82, GND83, GND84, GND85, GND86, GND87, GND88, GND89, GND90, GND91, GND92, GND93, GND94, GND95, GND96, GND97, GND98, GND99, GND100).
- Audio Components:** Includes a microphone (MIC), a speaker (SPK), and various capacitors (C3607, C3608, C3609, C3610, C3612, C3613, C3622, C3623, C3632, C3634, C3635, C3636, C3637, C3638, C3639, C3640, C3641, C3642, C3643, C3644, C3645, C3646, C3647, C3648, C3649, C3650, C3651, C3652, C3653, C3654, C3655, C3656, C3657, C3658, C3659, C3660, C3661, C3662, C3663, C3664, C3665, C3666, C3667, C3668, C3669, C3670, C3671, C3672, C3673, C3674, C3675, C3676, C3677, C3678, C3679, C3680, C3681, C3682, C3683, C3684, C3685, C3686, C3687, C3688, C3689, C3690, C3691, C3692, C3693, C3694, C3695, C3696, C3697, C3698, C3699, C3700, C3701, C3702, C3703, C3704, C3705, C3706, C3707, C3708, C3709, C3710, C3711, C3712, C3713, C3714, C3715, C3716, C3717, C3718, C3719, C3720, C3721, C3722, C3723, C3724, C3725, C3726, C3727, C3728, C3729, C3730, C3731, C3732, C3733, C3734, C3735, C3736, C3737, C3738, C3739, C3740, C3741, C3742, C3743, C3744, C3745, C3746, C3747, C3748, C3749, C3750, C3751, C3752, C3753, C3754, C3755, C3756, C3757, C3758, C3759, C3760, C3761, C3762, C3763, C3764, C3765, C3766, C3767, C3768, C3769, C3770, C3771, C3772, C3773, C3774, C3775, C3776, C3777, C3778, C3779, C3780, C3781, C3782, C3783, C3784, C3785, C3786, C3787, C3788, C3789, C3790, C3791, C3792, C3793, C3794, C3795, C3796, C3797, C3798, C3799, C3800, C3801, C3802, C3803, C3804, C3805, C3806, C3807, C3808, C3809, C3810, C3811, C3812, C3813, C3814, C3815, C3816, C3817, C3818, C3819, C3820, C3821, C3822, C3823, C3824, C3825, C3826, C3827, C3828, C3829, C3830, C3831, C3832, C3833, C3834, C3835, C3836, C3837, C3838, C3839, C3840, C3841, C3842, C3843, C3844, C3845, C3846, C3847, C3848, C3849, C3850, C3851, C3852, C3853, C3854, C3855, C3856, C3857, C3858, C3859, C3860, C3861, C3862, C3863, C3864, C3865, C3866, C3867, C3868, C3869, C3870, C3871, C3872, C3873, C3874, C3875, C3876, C3877, C3878, C3879, C3880, C3881, C3882, C3883, C3884, C3885, C3886, C3887, C3888, C3889, C3890, C3891, C3892, C3893, C3894, C3895, C3896, C3897, C3898, C3899, C3900, C3901, C3902, C3903, C3904, C3905, C3906, C3907, C3908, C3909, C3910, C3911, C3912, C3913, C3914, C3915, C3916, C3917, C3918, C3919, C3920, C3921, C3922, C3923, C3924, C3925, C3926, C3927, C3928, C3929, C3930, C3931, C3932, C3933, C3934, C3935, C3936, C3937, C3938, C3939, C3940, C3941, C3942, C3943, C3944, C3945, C3946, C3947, C3948, C3949, C3950, C3951, C3952, C3953, C3954, C3955, C3956, C3957, C3958, C3959, C3960, C3961, C3962, C3963, C3964, C3965, C3966, C3967, C3968, C3969, C3970, C3971, C3972, C3973, C3974, C3975, C3976, C3977, C3978, C3979, C3980, C3981, C3982, C3983, C3984, C3985, C3986, C3987, C3988, C3989, C3990, C3991, C3992, C3993, C3994, C3995, C3996, C3997, C3998, C3999, C4000).

C3609/C3610 must be  
2.2uF for Realtek

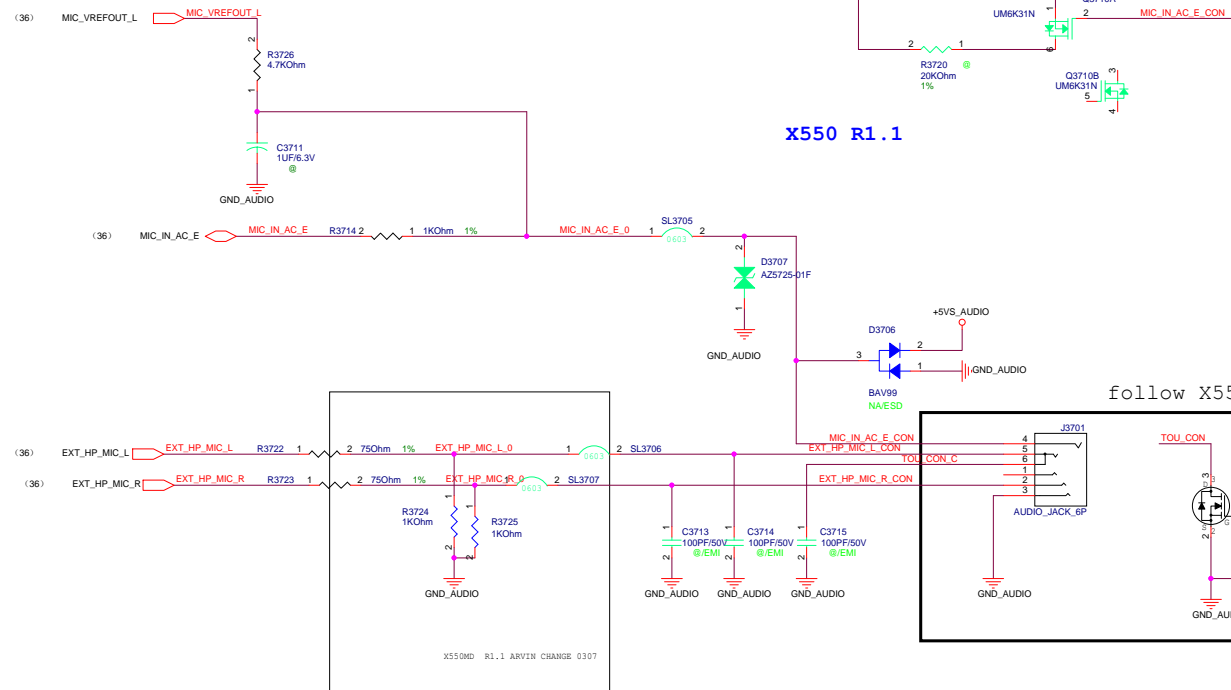


05/24:Interal MIC      RC Fliter

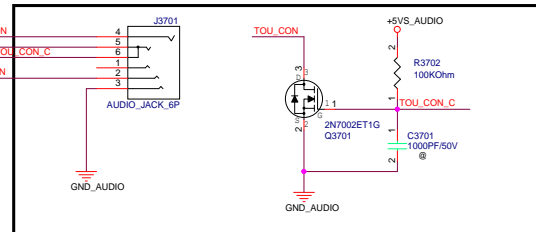
**X550 R2.0**

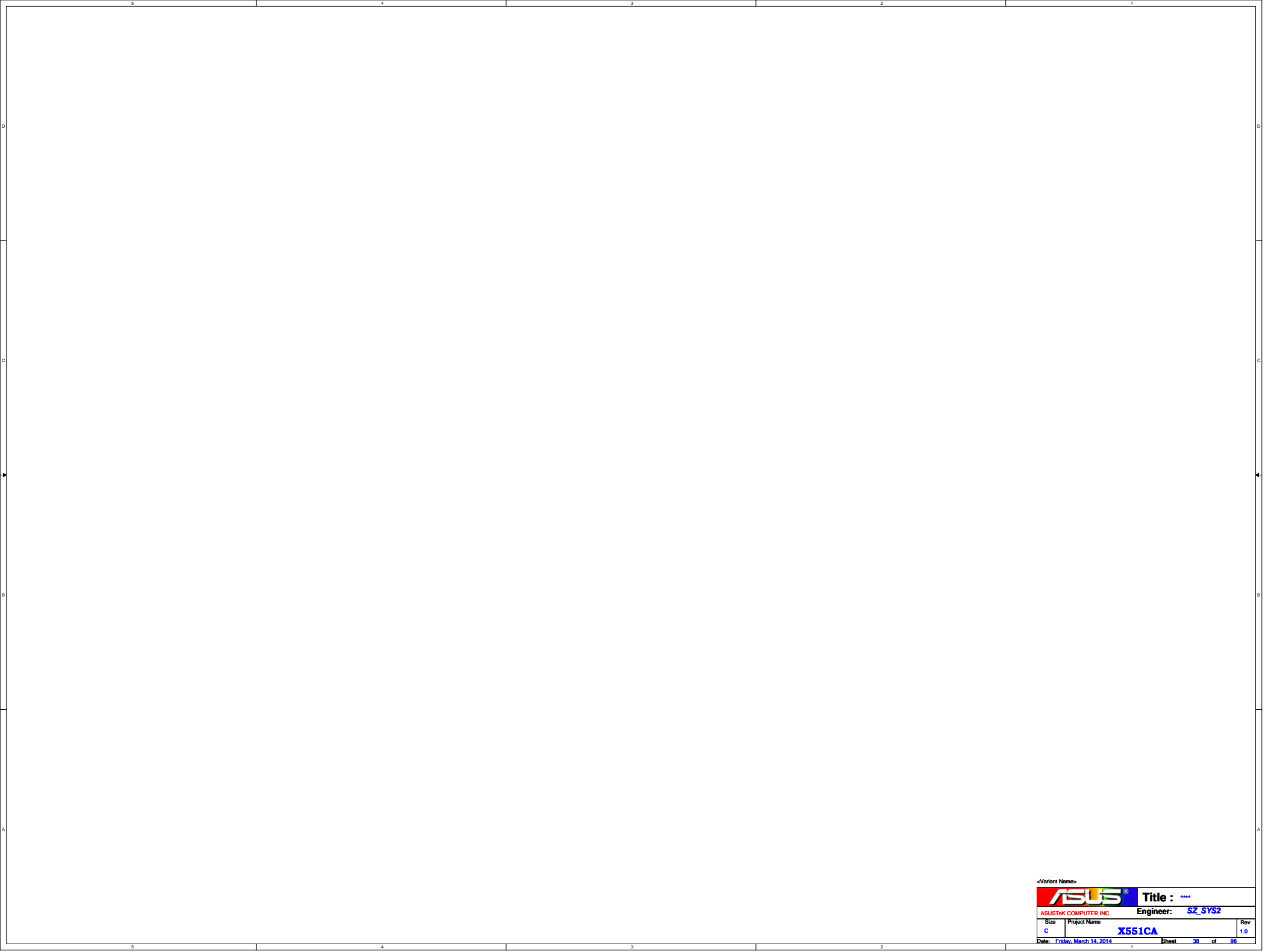


**X550 R1.1**



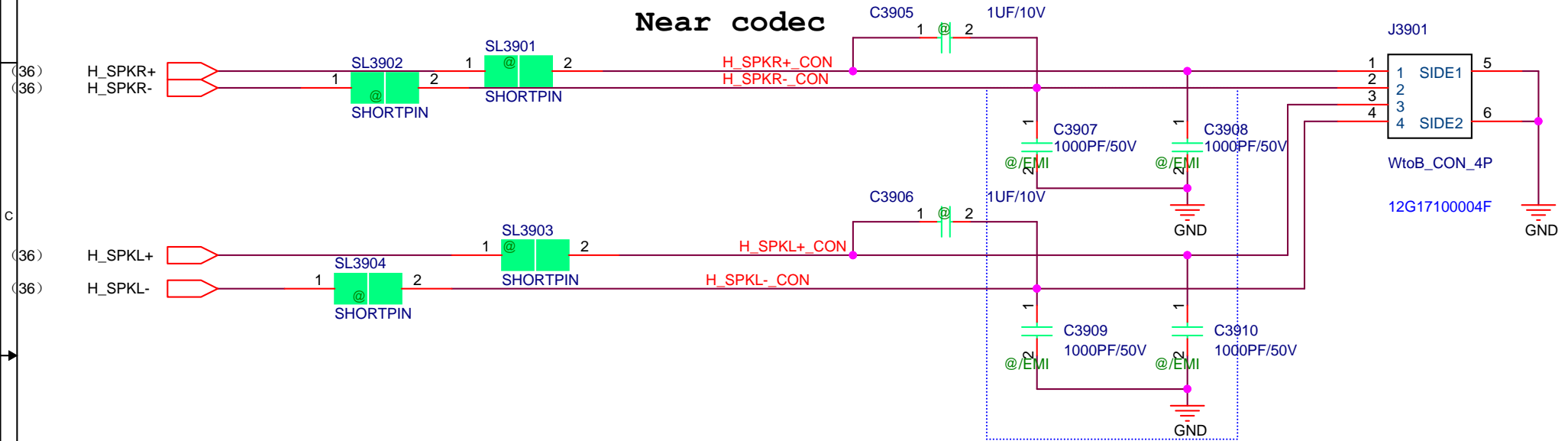
follow X550LD 140113






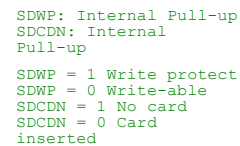
# Audio Speaker

## Near codec



		<b>Title :</b> AUD-SPEAKER CONN.	
ASUSTeK COMPUTER INC.		<b>Engineer:</b> SZ_SYS2	
Size A	Project Name <b>X551CA</b>		Rev 1.0
Date: Friday, March 14, 2014		Sheet 39 of 98	

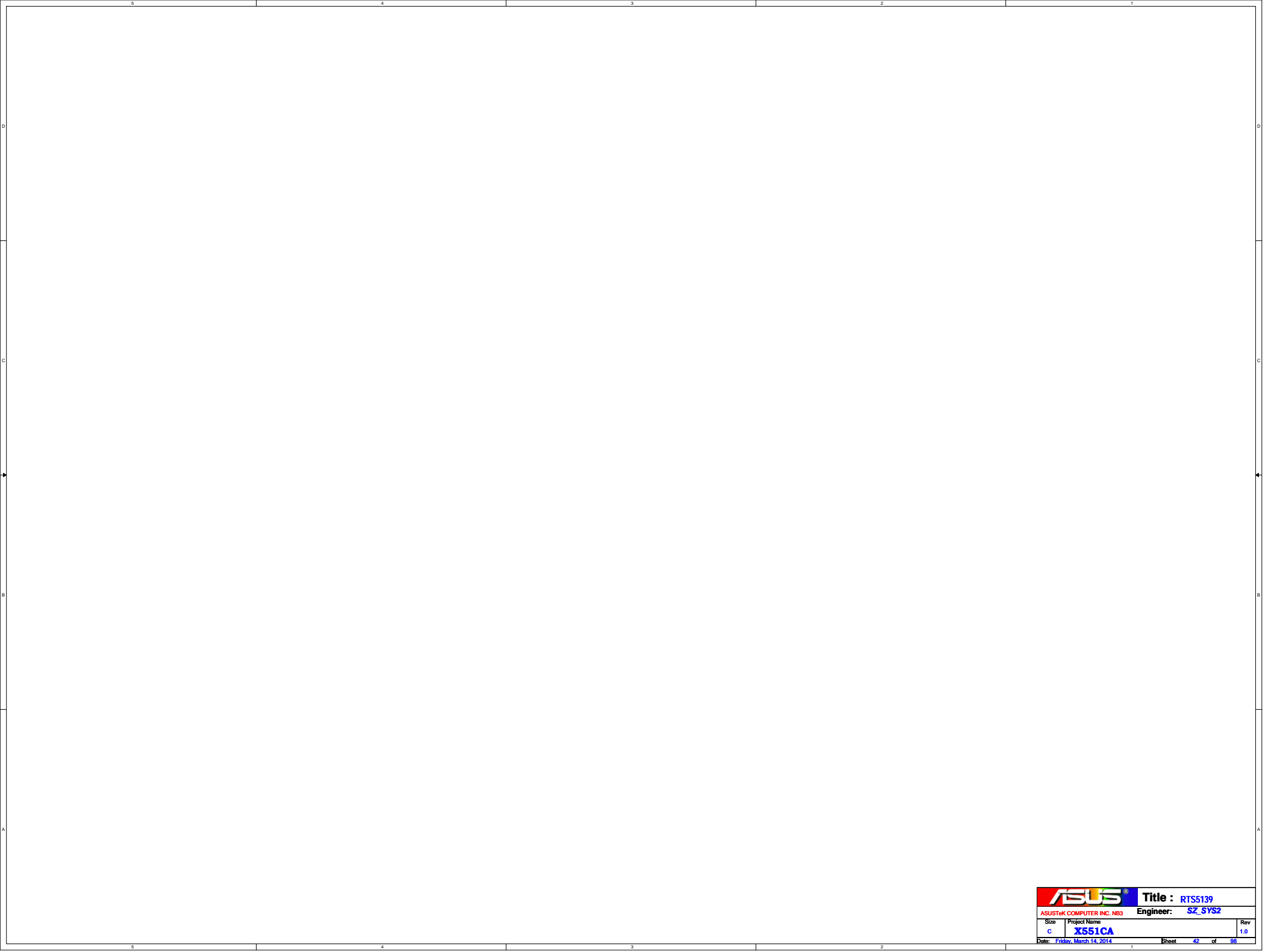
	A	B	C	D	E
1					
2					
3					
4					
5					

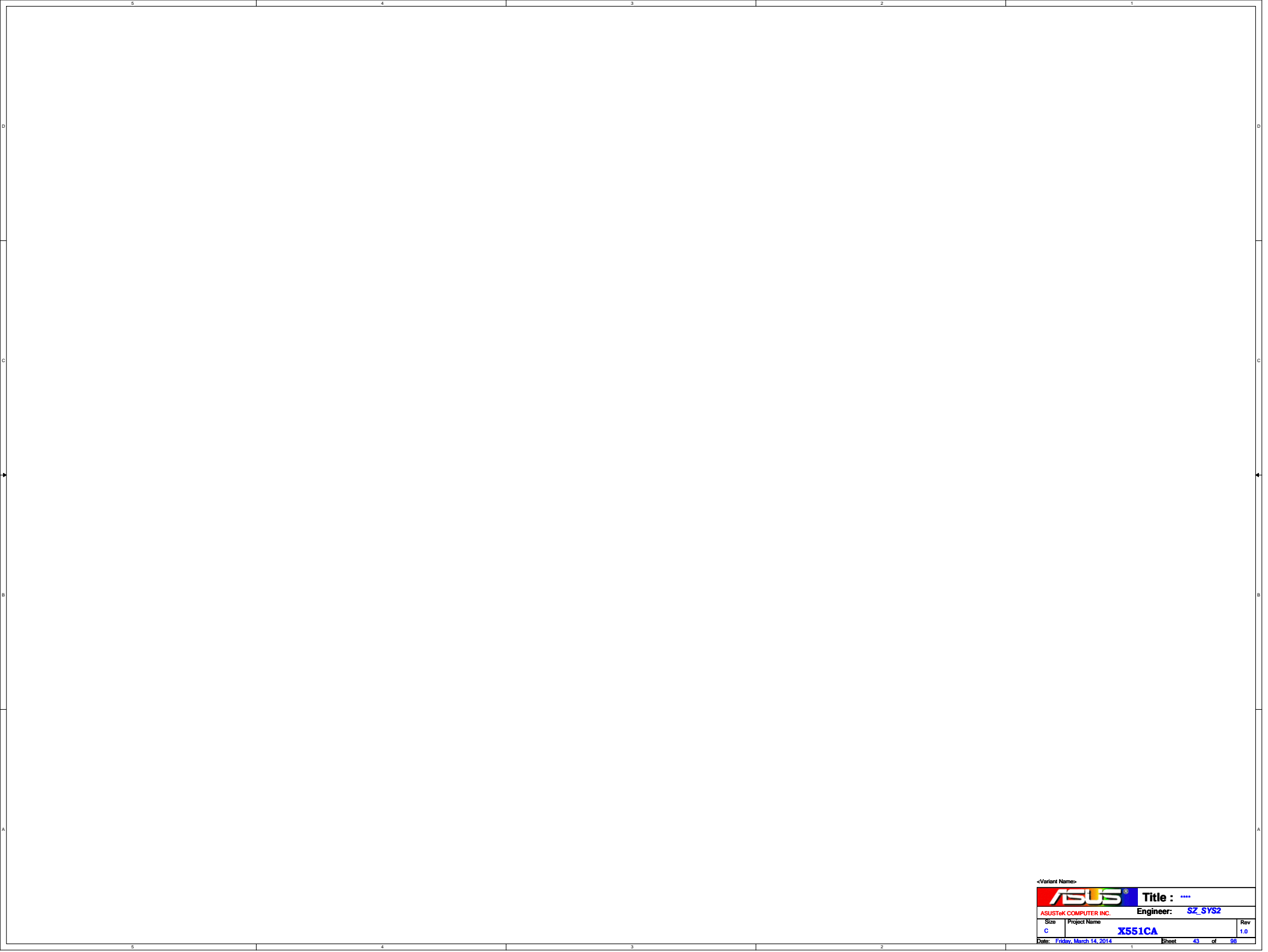


```
SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card
inserted
```



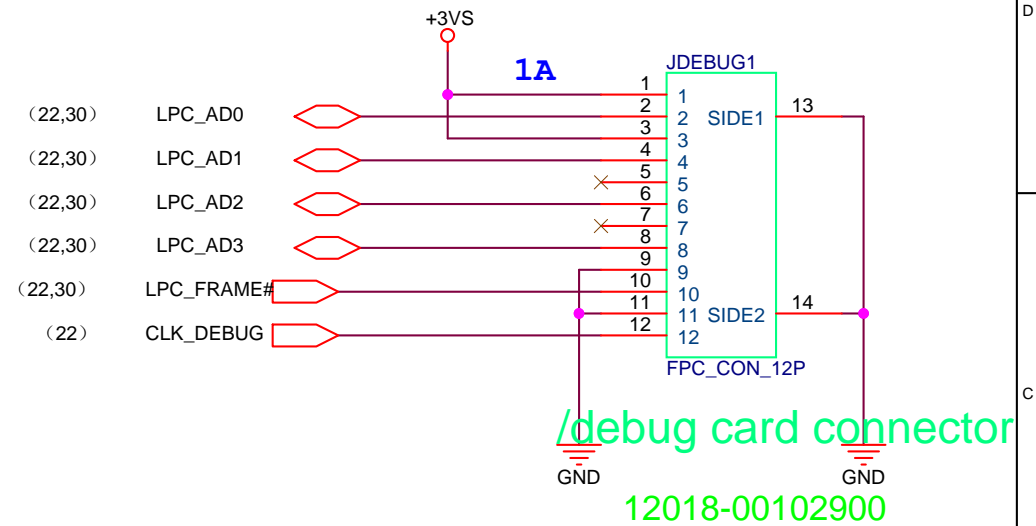
	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN







# LPC DEBUG PORT



LPC DEBUG PORT

TPM interface signals

LPC\_AD0

LPC\_AD1

LPC\_AD2

LPC\_AD3

LPC\_FRAME#

+3V

LPCPD#

INT\_SERIRQ

BUF\_PLT\_RST#

CLK\_33M\_TPM

TPM\_CLKRUN#

+3VS



Title : **DEBUG PORT**

ASUSTeK COMPUTER INC.

Engineer: **SZ\_SYS2**

Size

**A**

Project Name

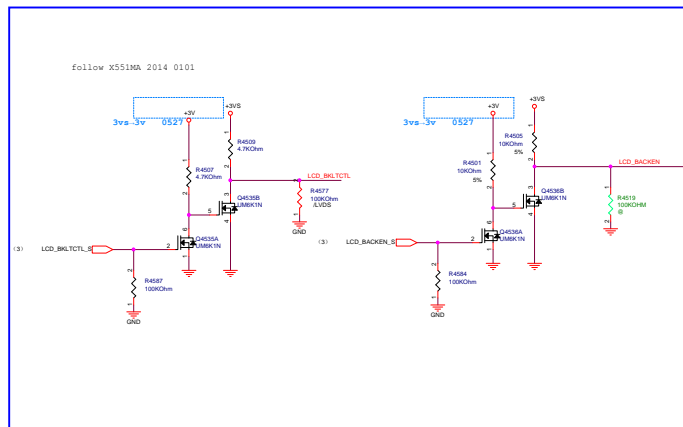
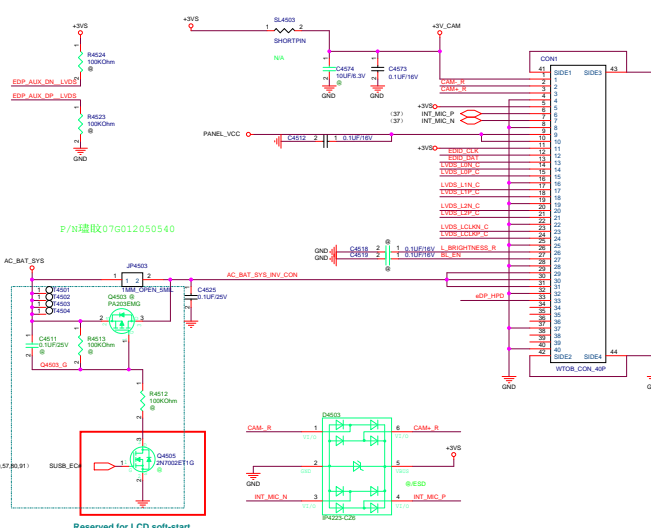
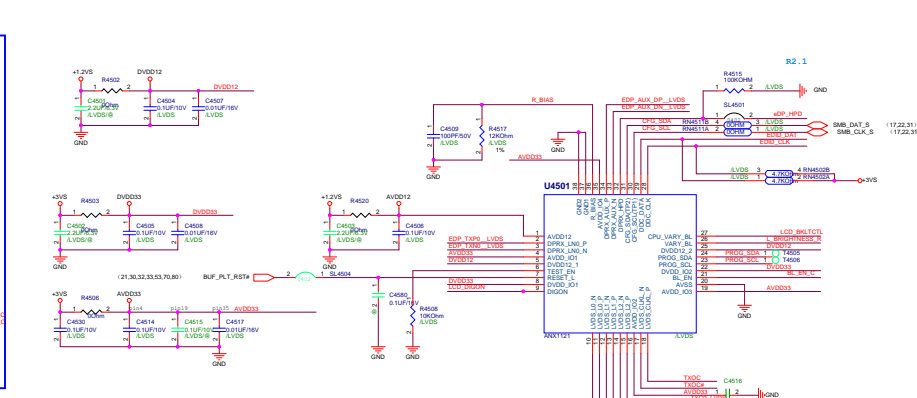
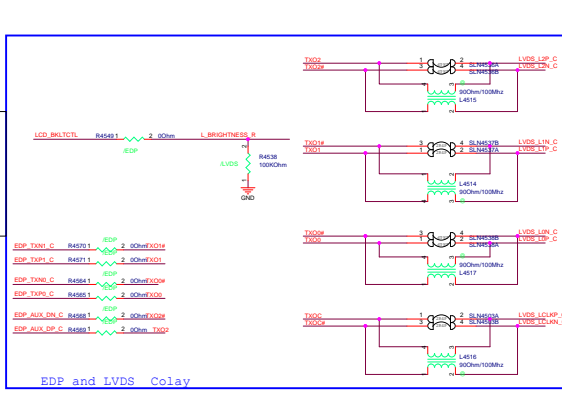
**X551CA**

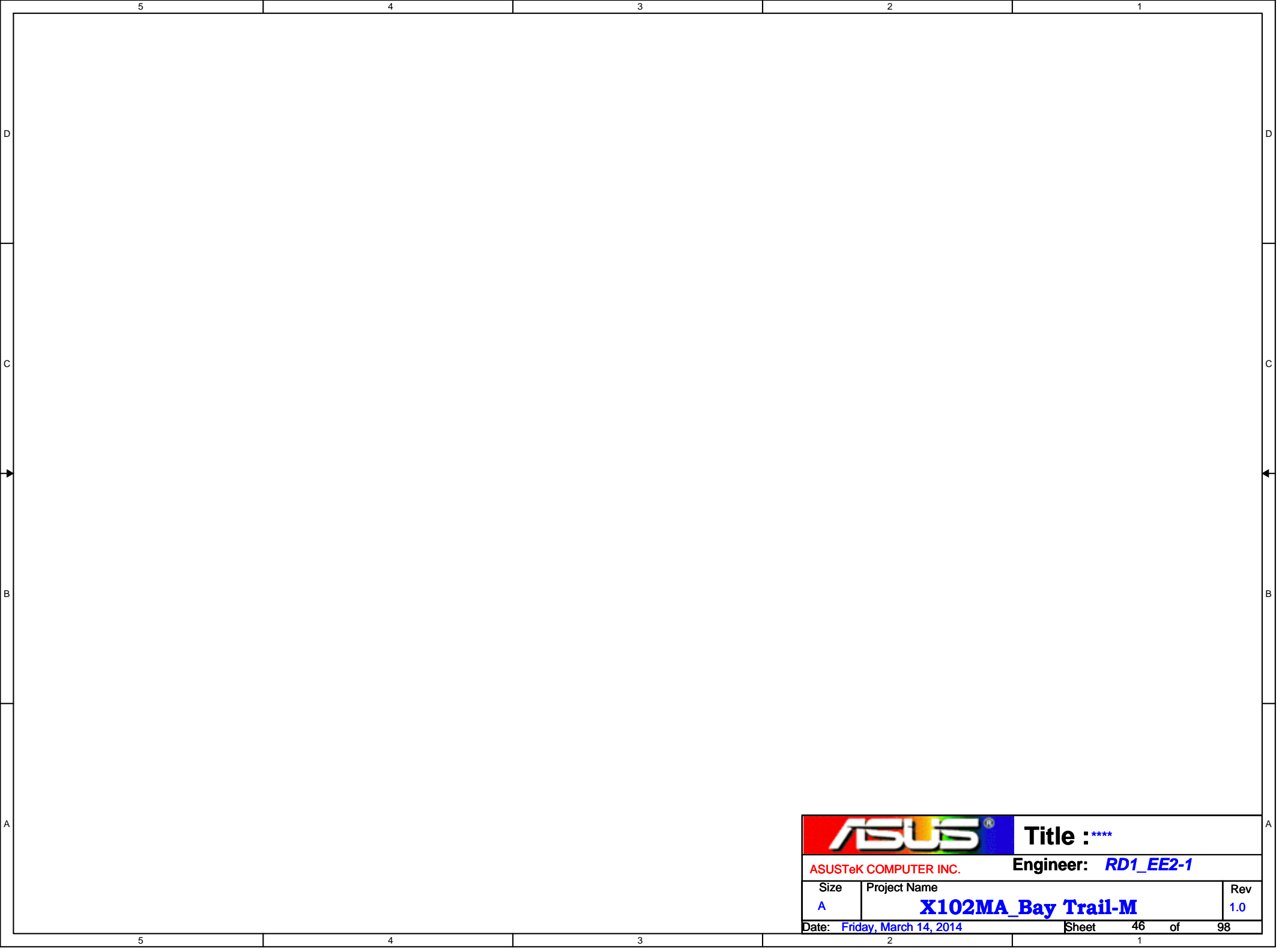
Rev


**1.0**

Date: **Friday, March 14, 2014**

Sheet **44** of **98**



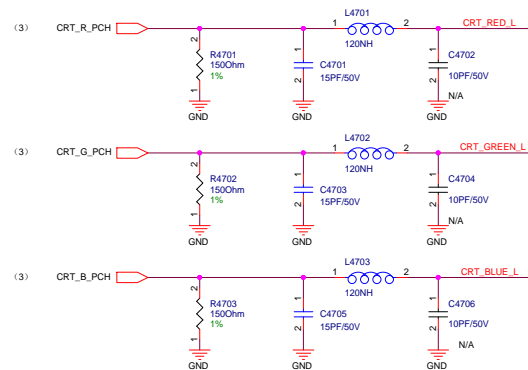


		Title : ****	
ASUSTeK COMPUTER INC.		Engineer: RD1_EE2-1	
Size A	Project Name X102MA_Bay Trail-M		Rev 1.0
Date: Friday, March 14, 2014		Sheet	46 of 98

# DAC Signal

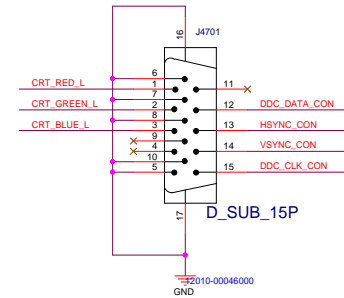
2nd source:  
09G023152003  
09G023152202  
09G023152500

BOM Mount: 09G023152401



follow X550LD

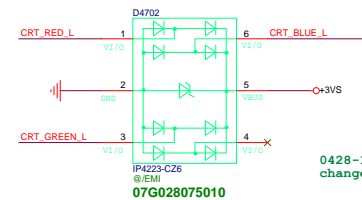
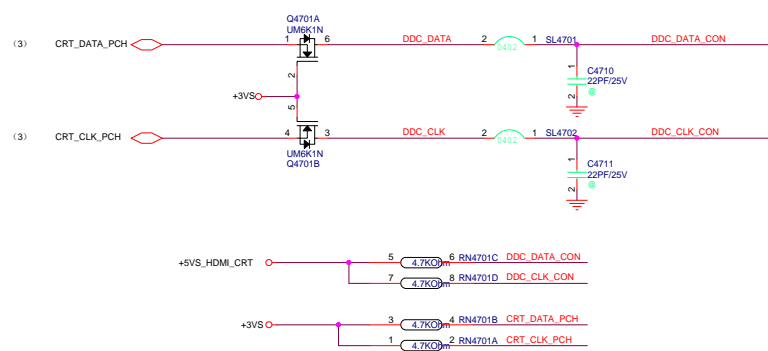
## CRT Connector



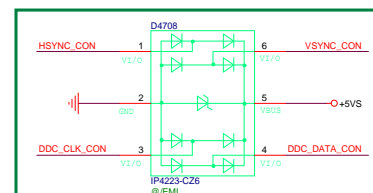
# SYNC Signal



# Control Signal



0428-1 EMI D3401, D3402, D4702, D5201, PD6001  
change P/N to 07G028176010





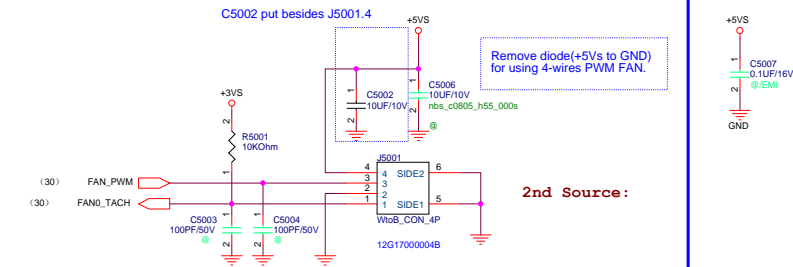


BOM

		Title : ****	
ASUSTeK COMPUTER INC		Engineer: RD1_EE2-1	
Size	Project Name		Rev
B	X102MA_Bay Trail-M		1.0
Date: Friday, March 14, 2014		Sheet	49 of 98

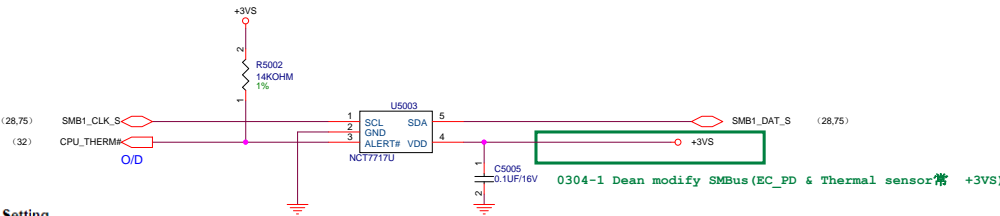
GPU Thermal Sensor

PWM Fan



CPU Thermal Sensor

R5002:14Kohm-->2Kohm  
Baytrail Tj,max = 75degC (reason: Tj-sdp = 80degC)



5.3 Address Setting

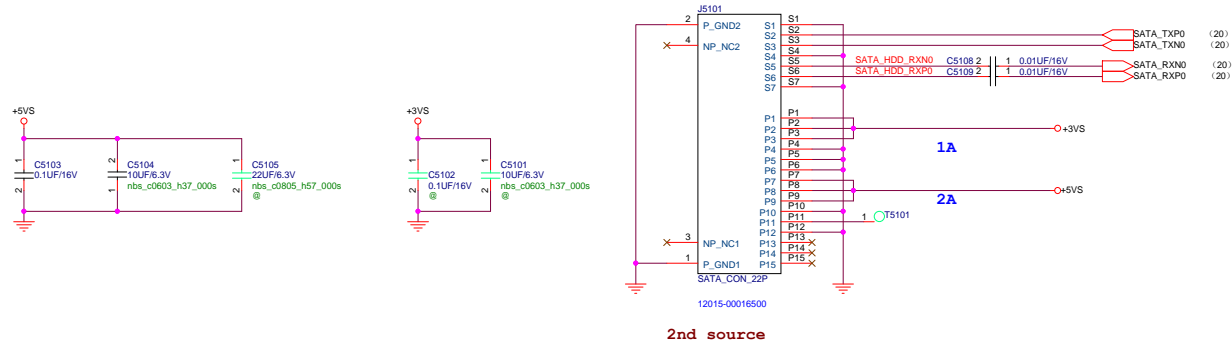
NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

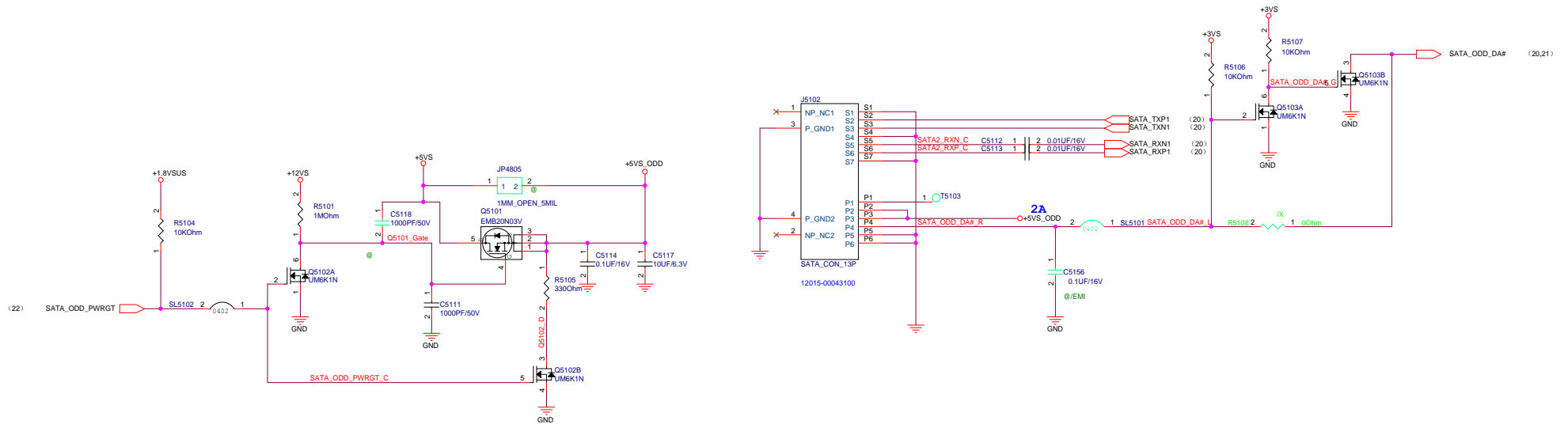
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

## SATA HDD



## SATA ODD

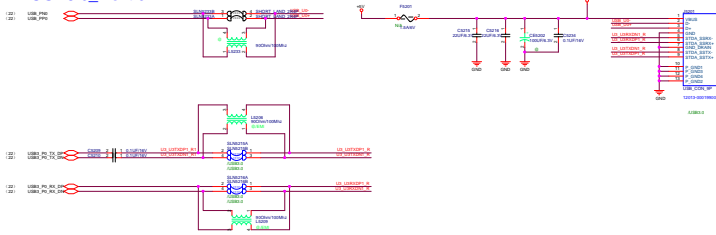




X552MD

### USB3.0\_Port 0

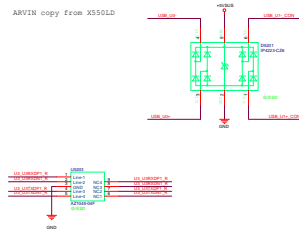
ARVIN copy from X550LD



X552MD

### ESD-Protection

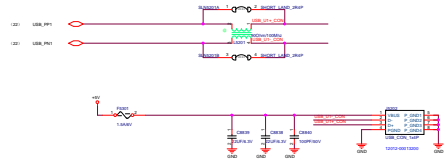
ARVIN copy from X550LD



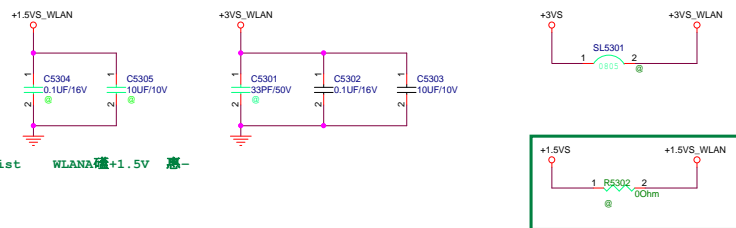
X552MD

### USB2.0\_Port 1

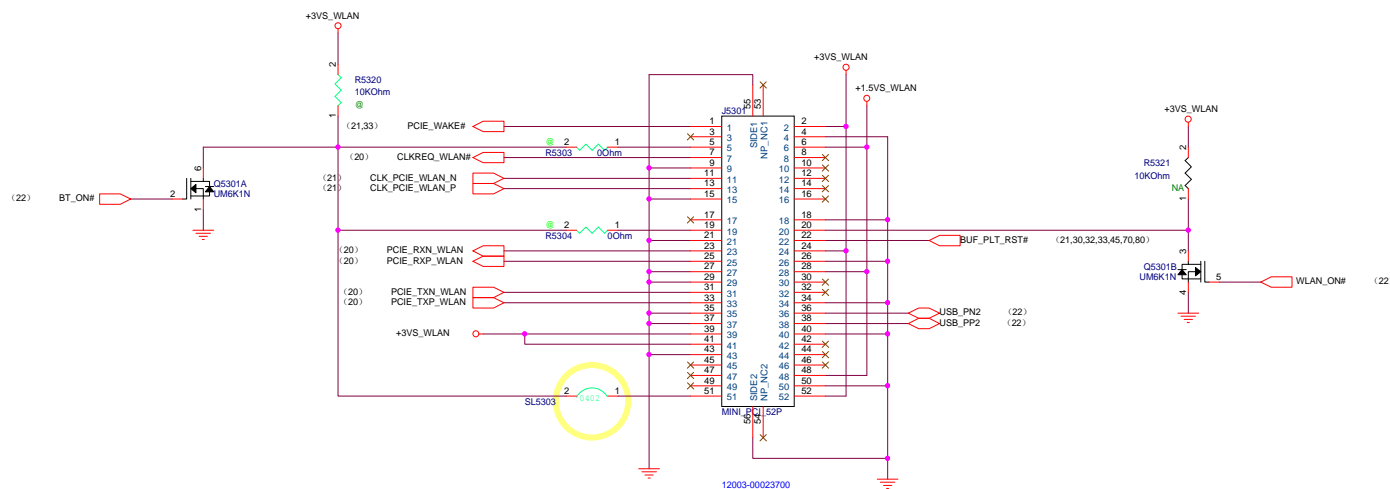
ARVIN copy from X550LD



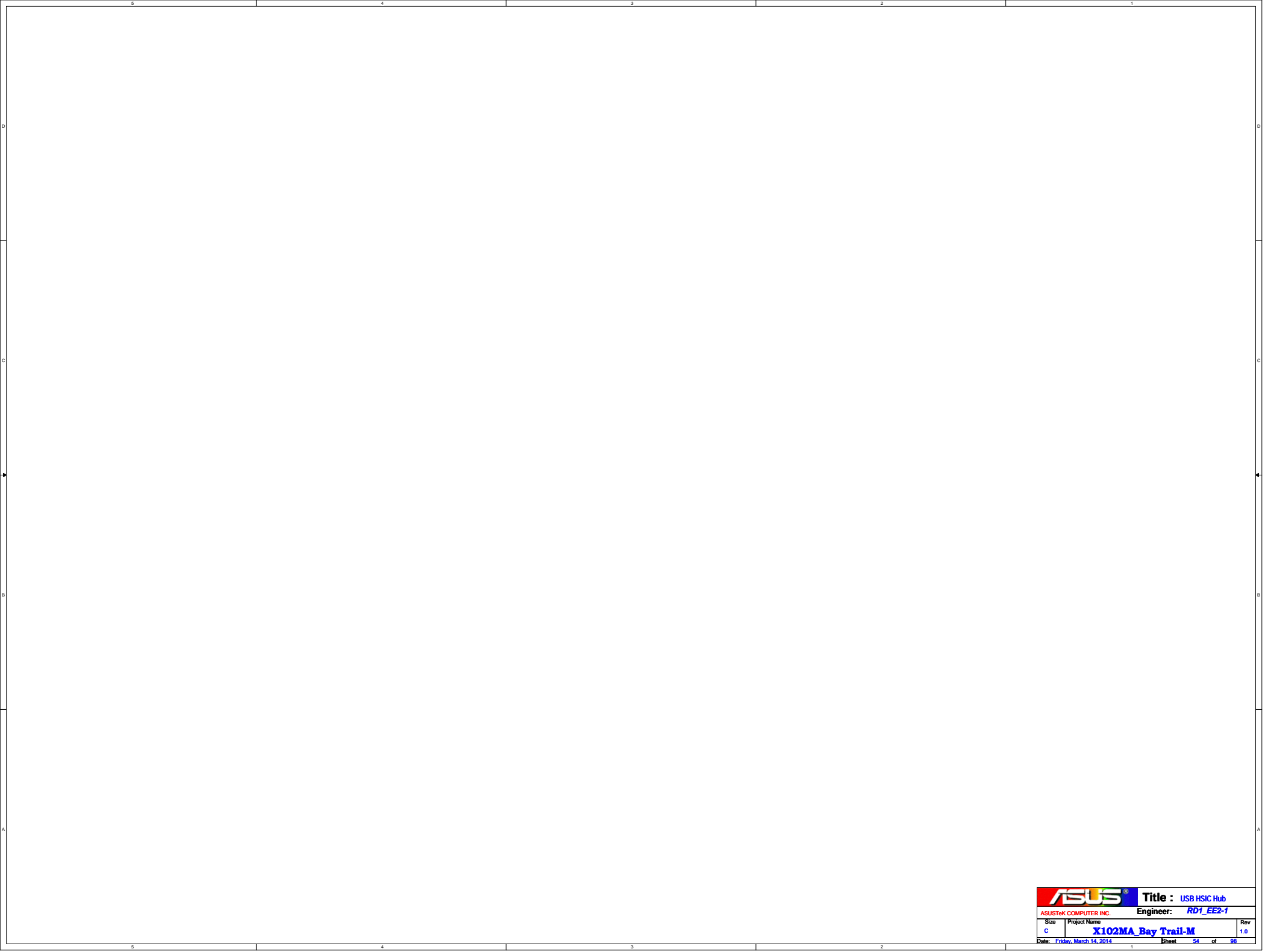
0520-11 Dean Merge BOM L3000 L5301 L2603 L2604 L2707  
=> 1200HM/2A 09G013120802



0309-11 Dean cost check keypart list WLANA端+1.5V 意-  
=> unstuff C5304, C5305




2nd source:  
12003-00024000





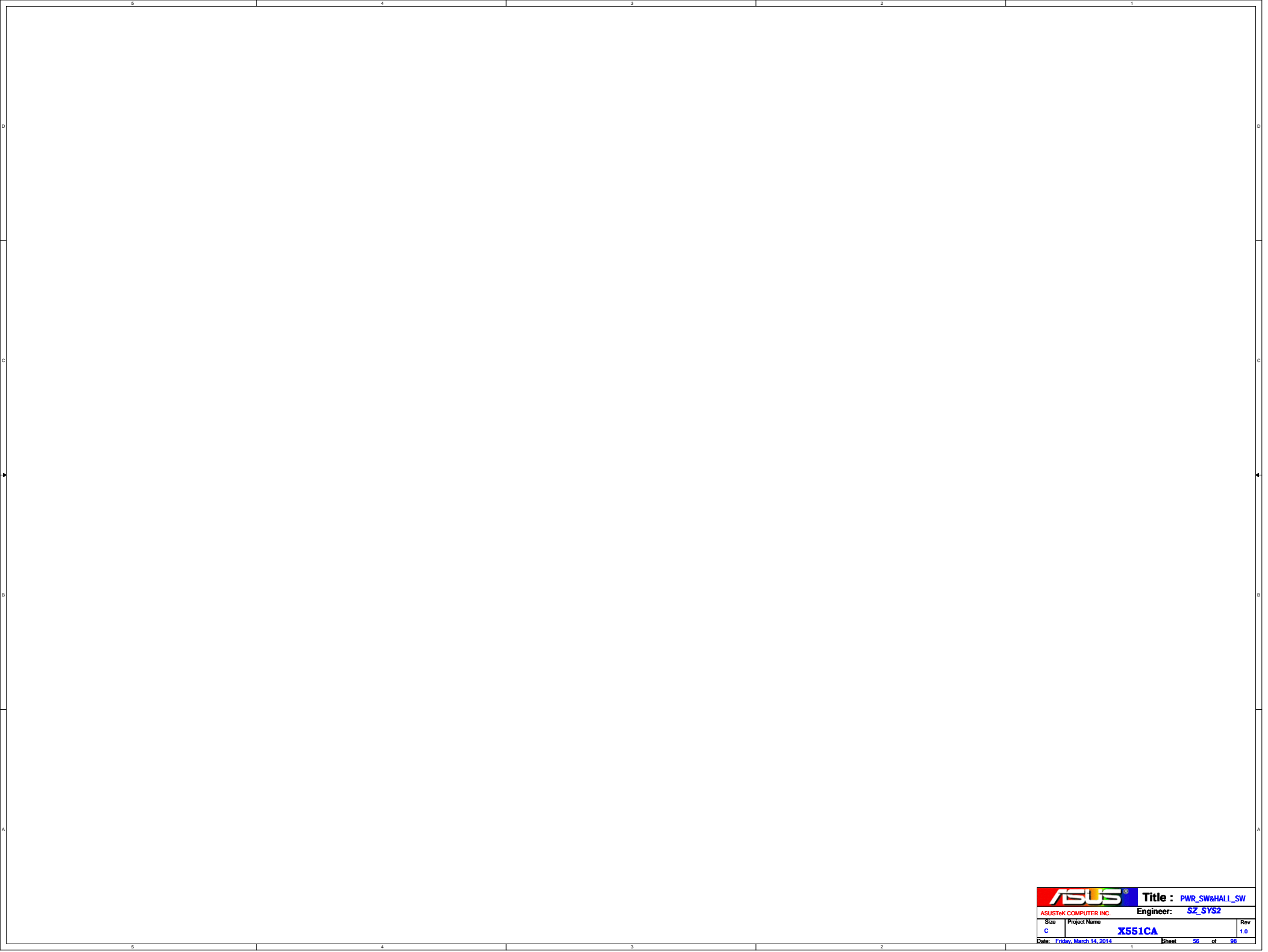
<Variant Name>

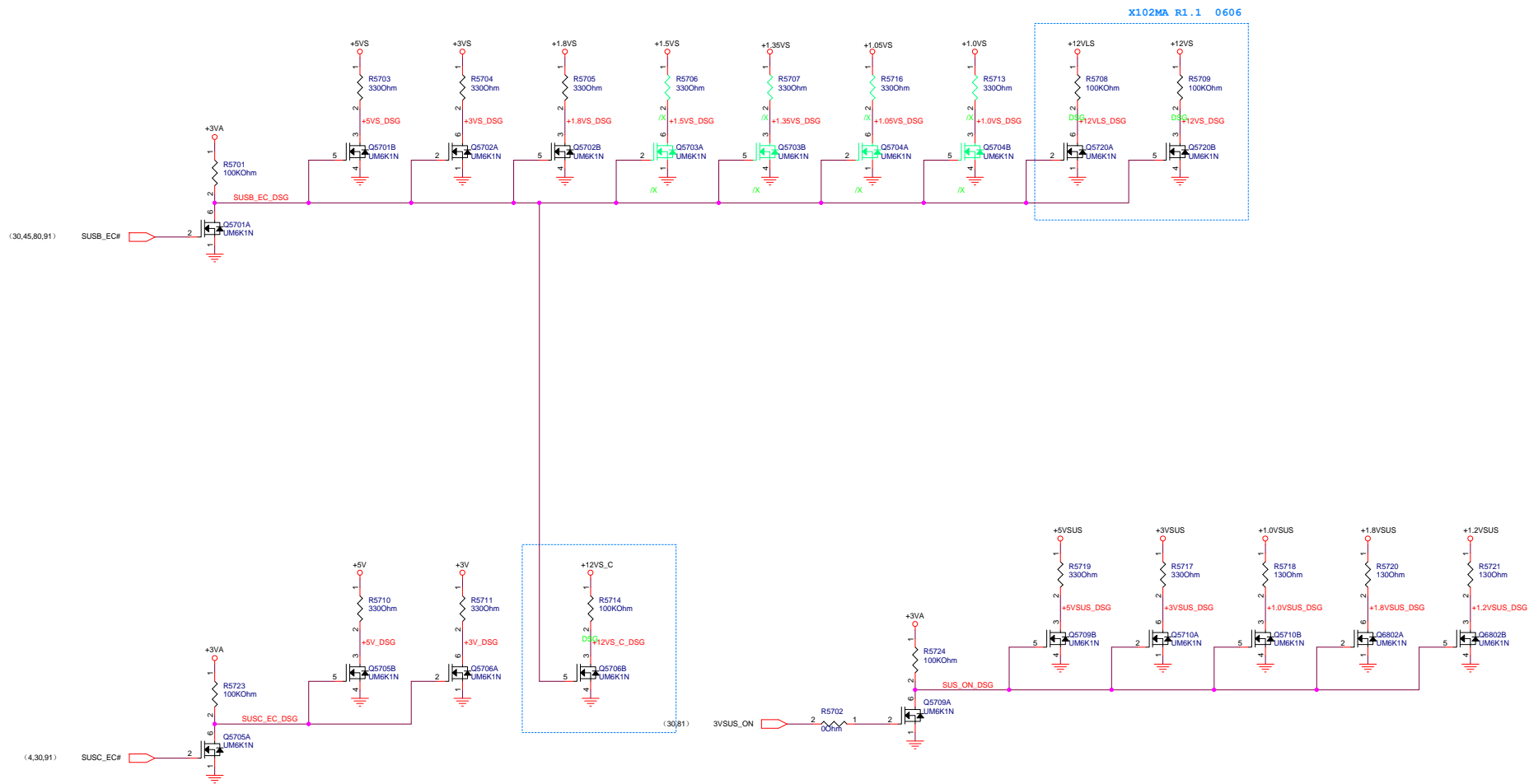
**Title :** NFC

ASUSTeK COMPUTER INC. NB8**Engineer:** RD1\_EE2-1

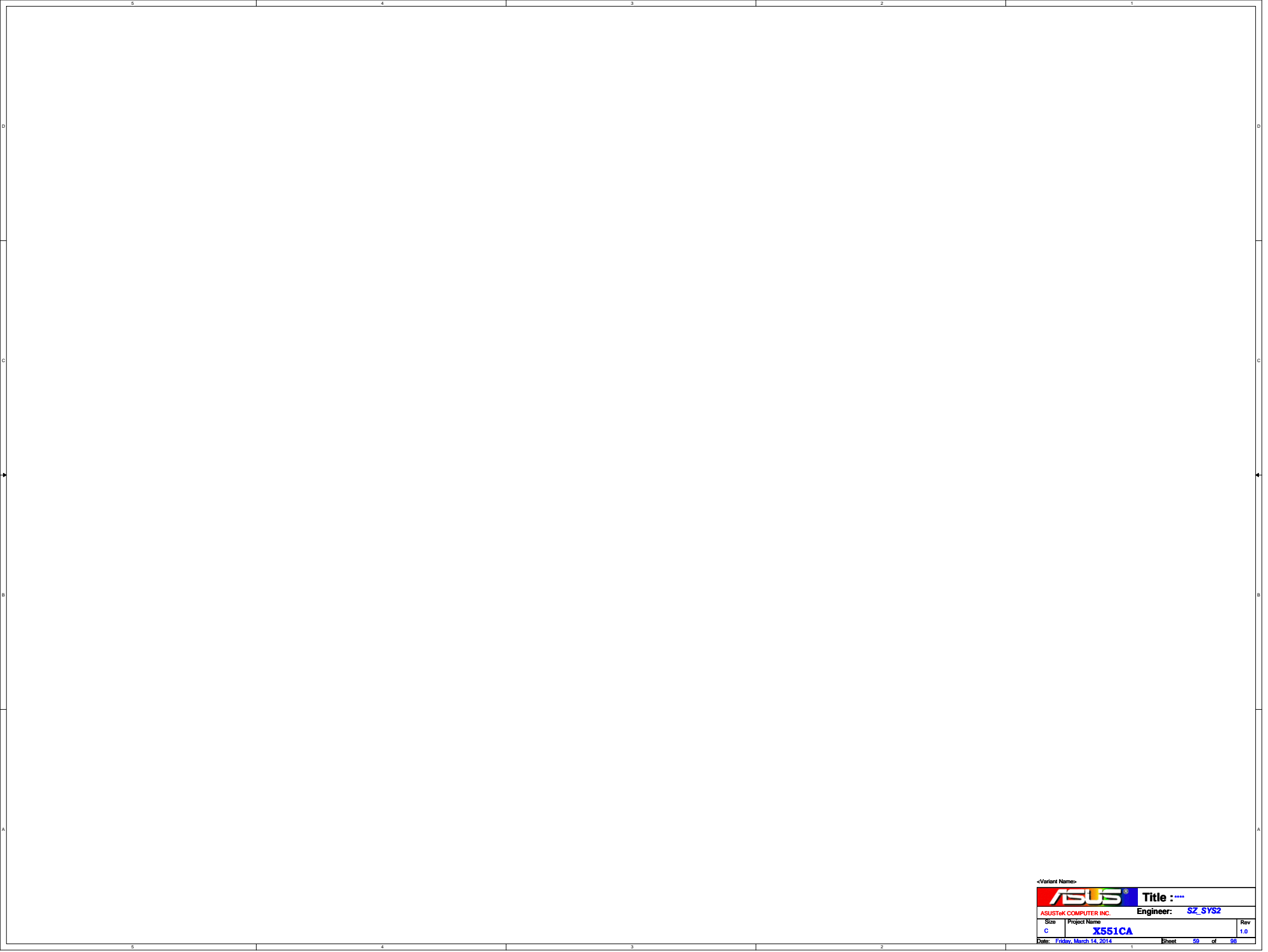
Size	Project Name	Rev
A3	<b>X102MA Bay Trail-M</b>	1.0

Date: Friday, March 14, 2014Sheet 55 of 98

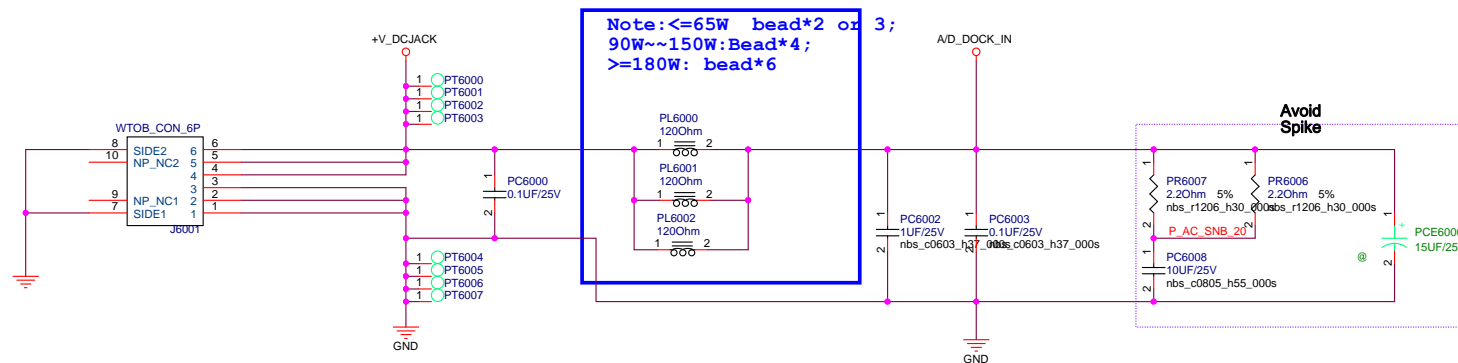












## Battery Connector

BAT\_CON 婉 pin3 叫 NC, 1 璫锁 GND.

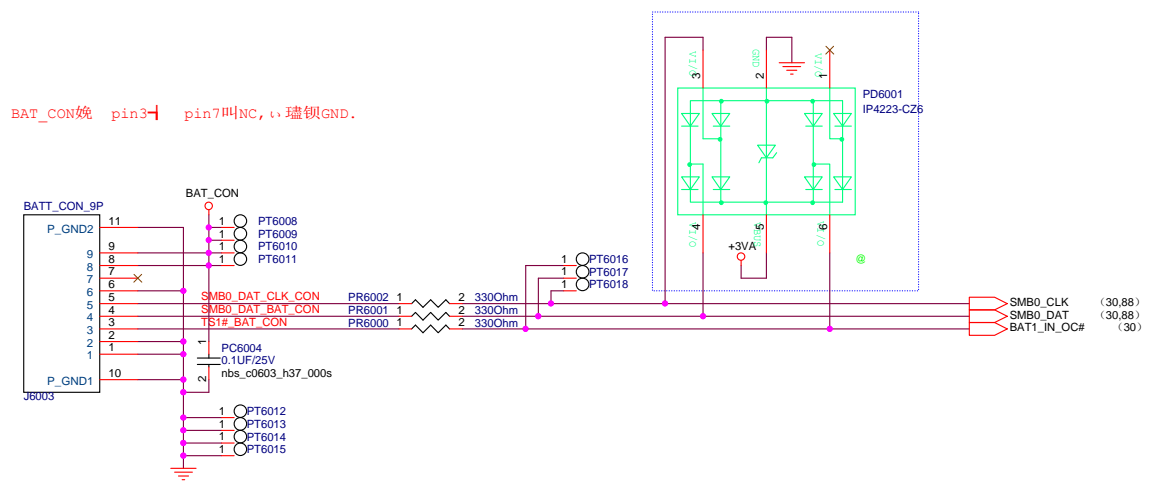




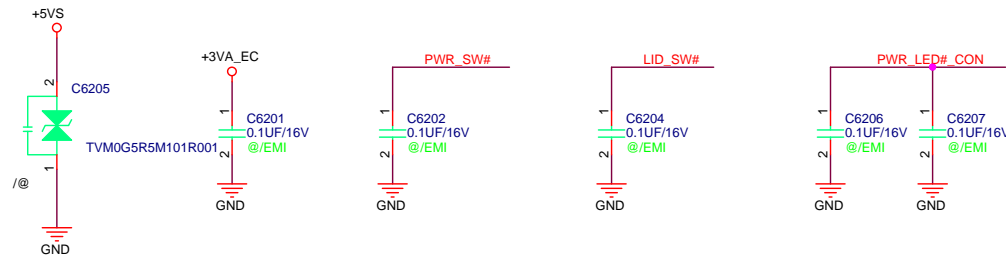
Diagram illustrating the connection of the J6201 module. The module is connected to a power source (3VA\_EC, +5VS) and ground (GND). The module is also connected to a 2nd source (12G18340060W) via a 12018-00160200 cable. The module is labeled J6201.

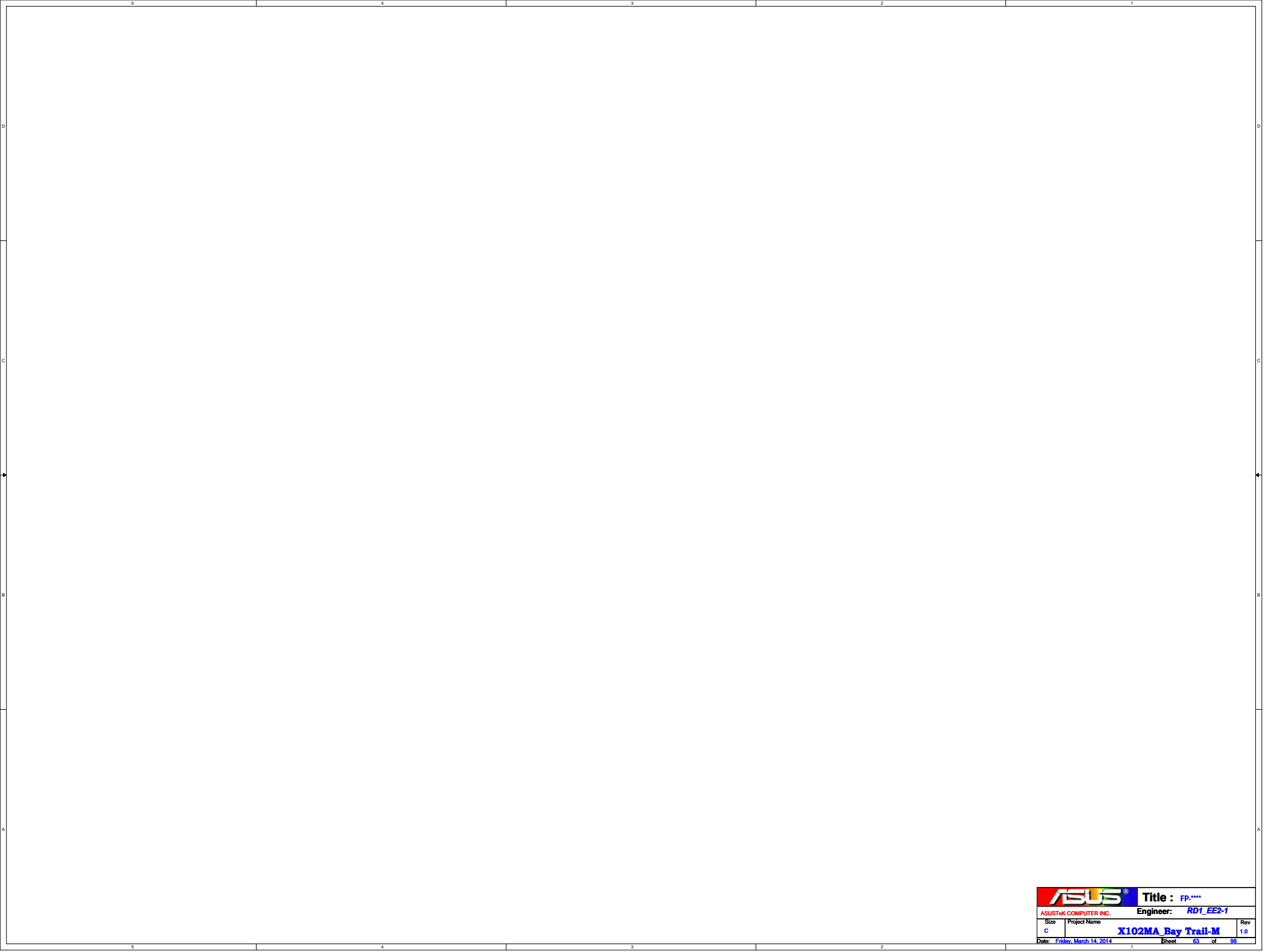
Pin connections for J6201:

- Pin 1: SIDE1
- Pin 2: 1
- Pin 3: 2
- Pin 4: 3
- Pin 5: 4
- Pin 6: SIDE2
- Pin 7: FPC\_CON\_6P
- Pin 8: 8

External connections:

- 3VA\_EC
- +5VS
- (30) PWR\_SW#
- (67) PWR\_LED#\_CON
- (30) LID\_SW#
- GND
- 12018-00160200
- 2nd source: 12G18340060W
- GND





# UART Debug Board



**Title :** UART Debug Board

ASUSTeK COMPUTER INC.

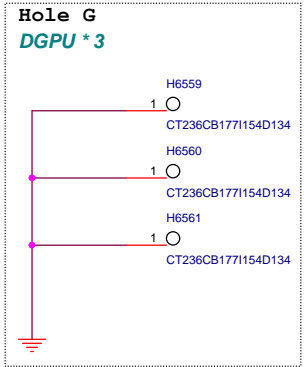
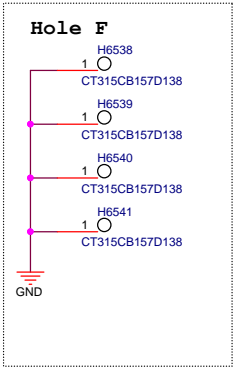
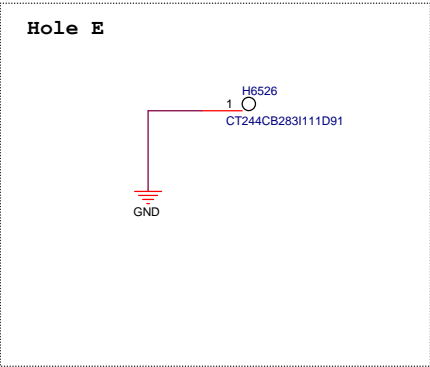
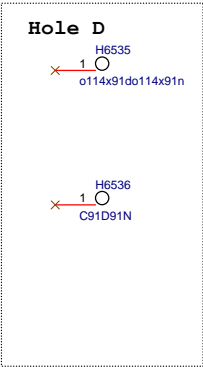
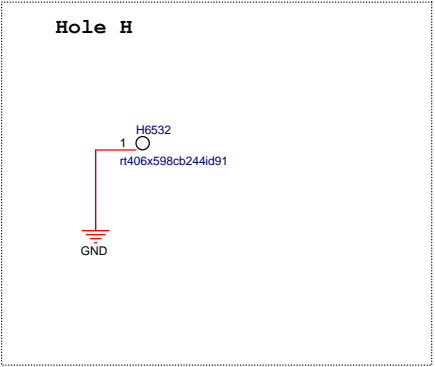
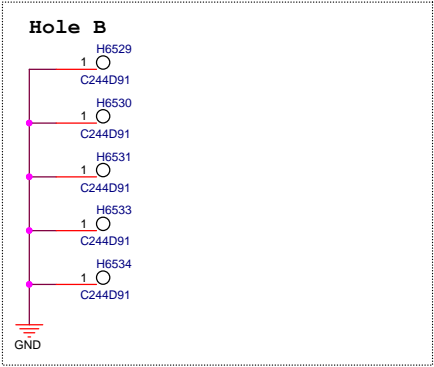
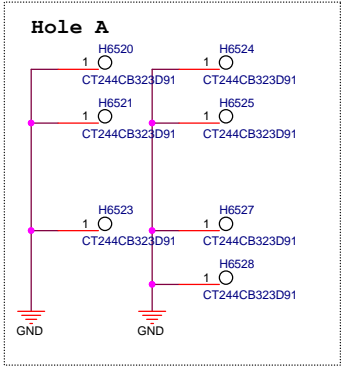
**Engineer:** RD1\_EE2-1

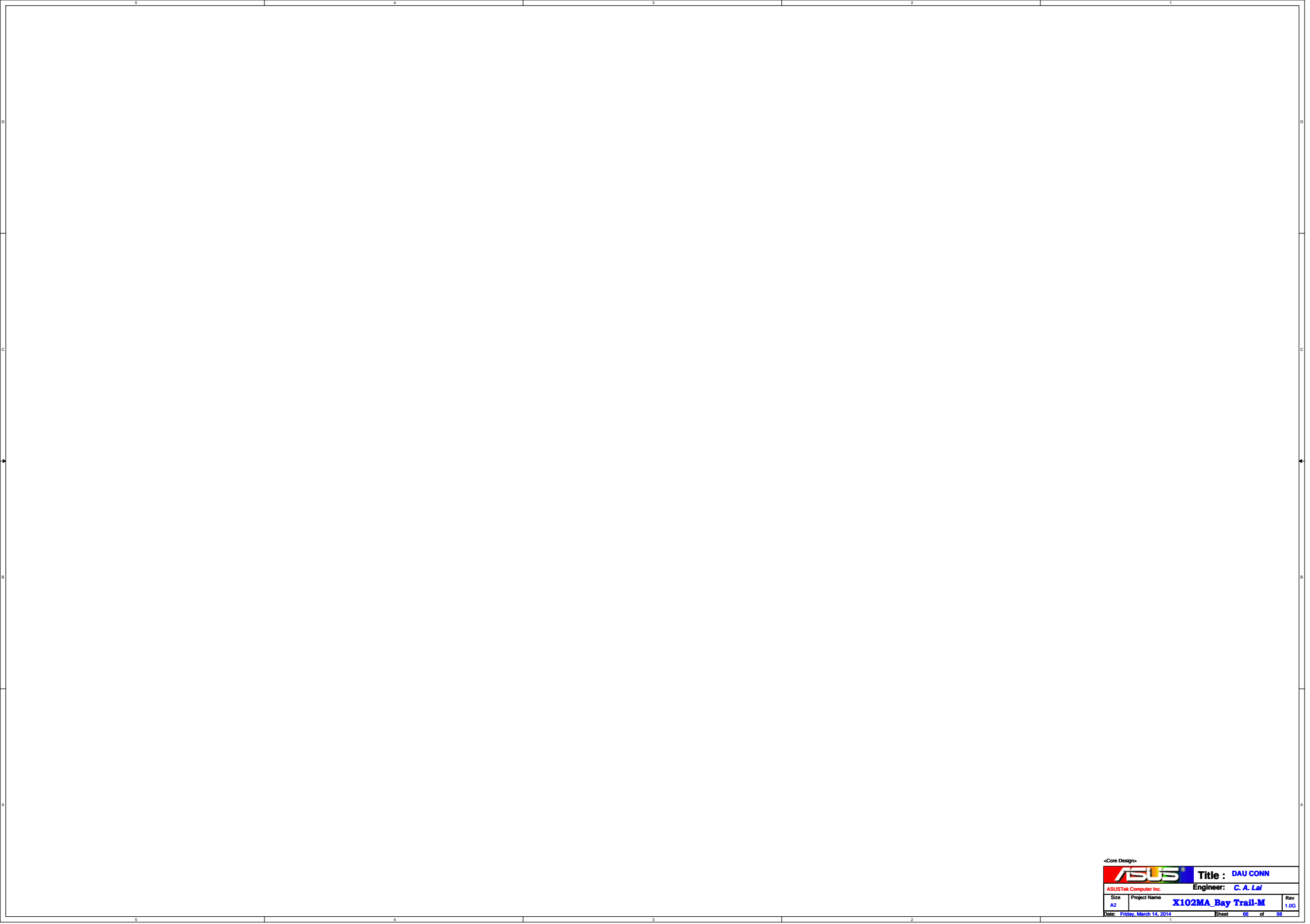
Size	Project Name	Rev
B	X102MA_Bay Trail-M	1.0

Date: Friday, March 14, 2014

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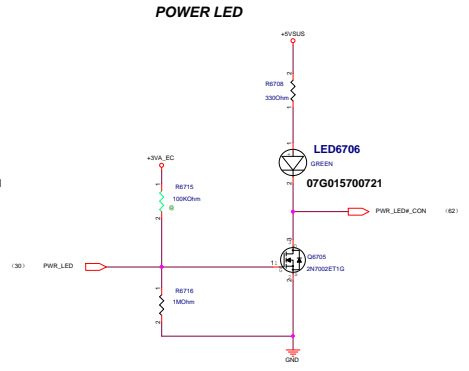
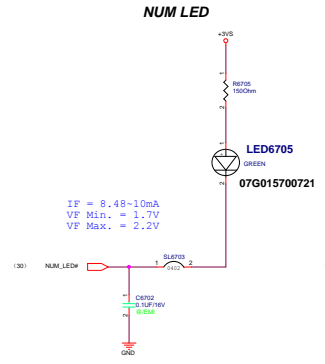
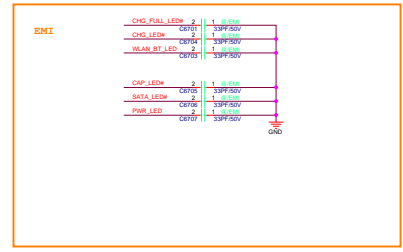
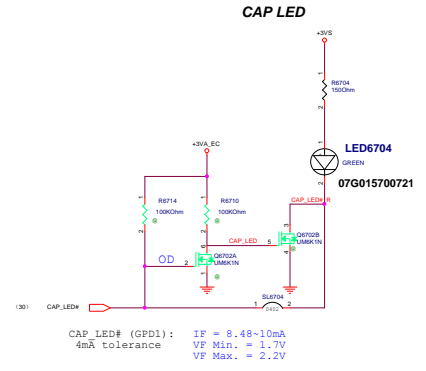
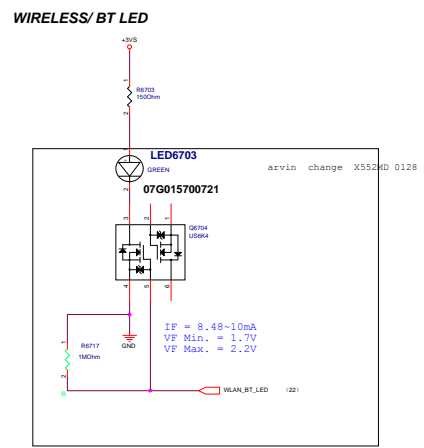
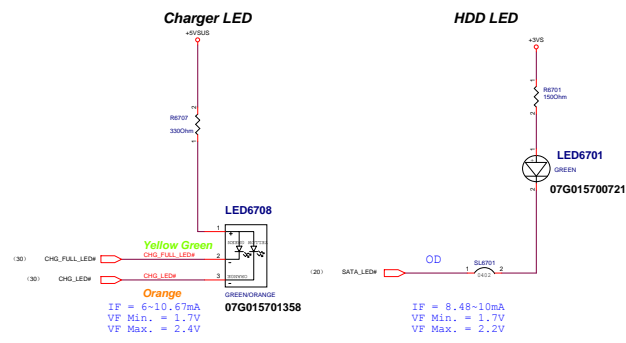
Screw Hole & SMT Nut



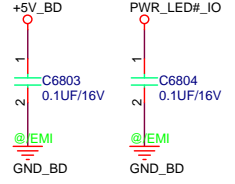
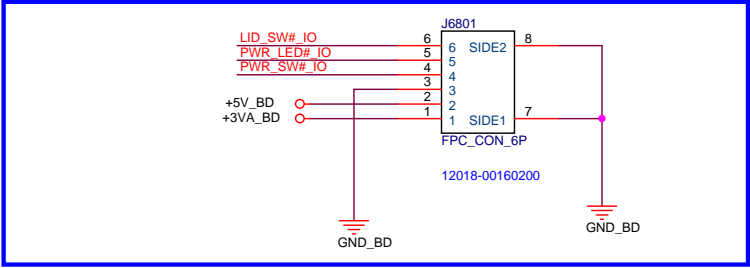
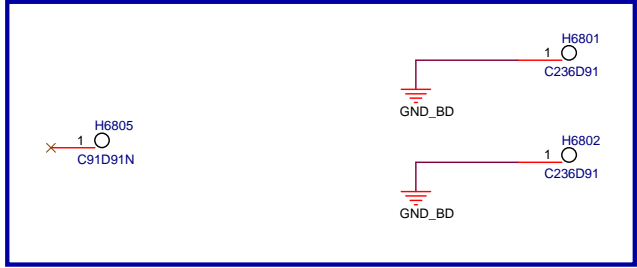
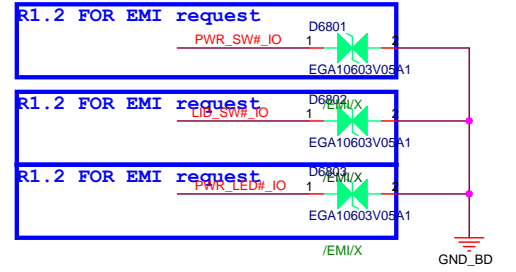
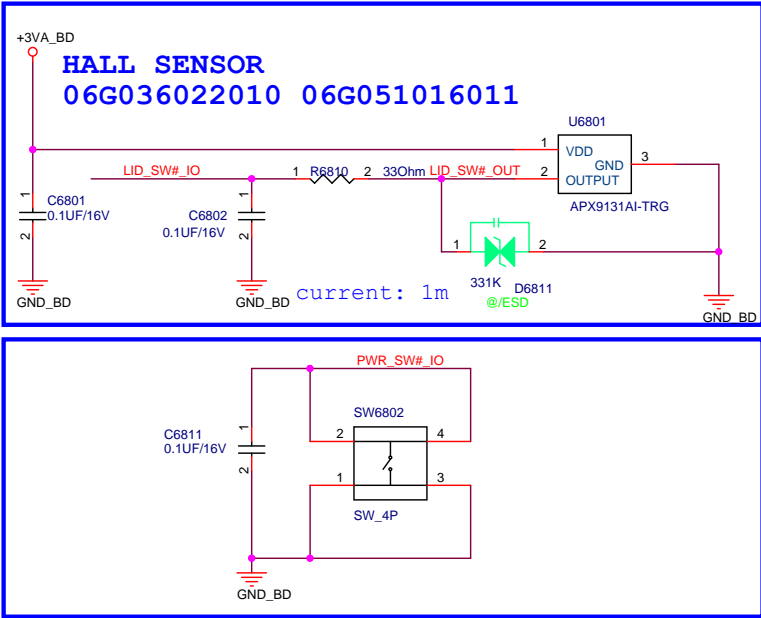
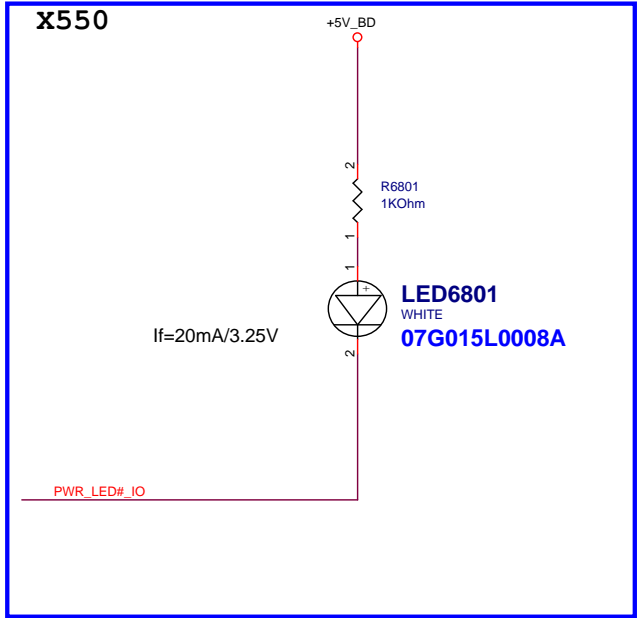


5	4	3	2	1
D				
C				
B				
A				

LED indicator







D

D

C

C

B

B

A

A



**Title :** EMI

ASUSTeK COMPUTER INC.

Engineer: **SZ\_SYS2**

Size  
A

Project Name	<b>X551CA</b>
--------------	---------------

Rev
1.0

Date: Friday, March 14, 2014

Sheet 69 of 98

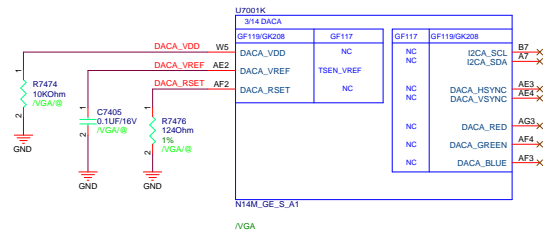




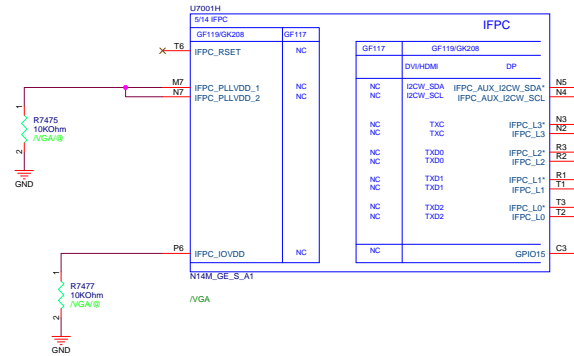




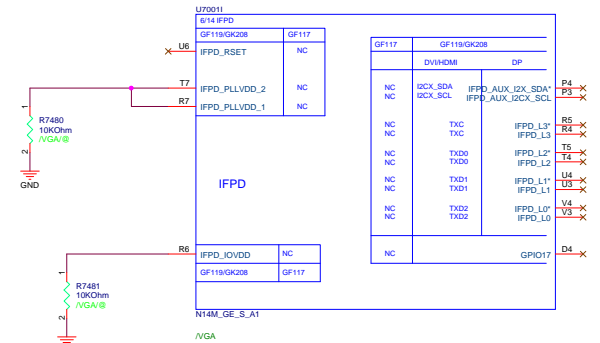
## CRT DAC\_A



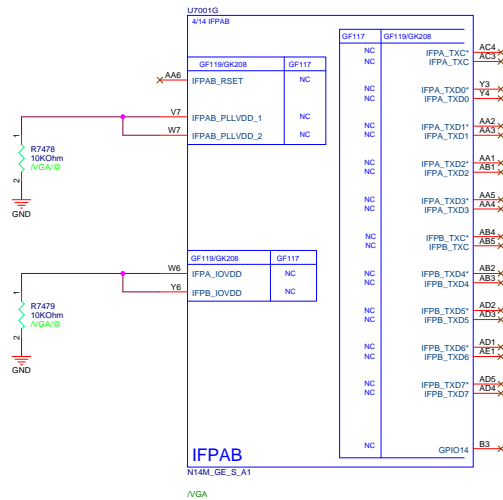
## DP(link C)



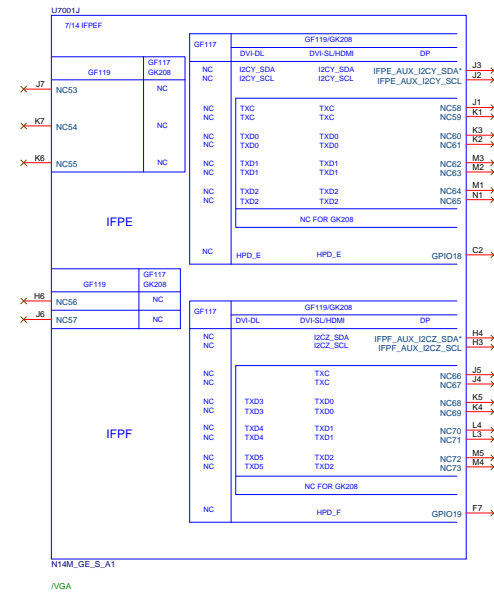
## DVI(link D)



## LVDS IFPA/B



## LVDS IFPE/F



<Variant Name>

Table 12-1. G528-64 and G548-128 GPIO Description

Pin Name	Normal Function	IO	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MCH	I	FB Clamp monitor for GC6 1.0	10K pull-down to GND
GPIO1	GC6_FB_EH	O	FB Enable for GC6 2.0	10K pull-up to 3V3_AON
GPIO2	MEM_VDD_CTL	O	Memory VDD VDD	10K pull-up to 3V3_AON
GPIO3	LC0D_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO4	LC0D_VCC	O	Panel Power Enable	100K pull-down
GPIO5	LC0D_BL_EN	O	Panel Backlight Enable	100K pull-down
GPIO6	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO7	FB_CLAMP_TGL_REQ	O	Clamp trigger request for GC6 1.0	10K pull-up to system 3.3V
GPIO8	GPU_EVENT#	I	GPU event input for GC6 2.0	10K pull-up to 3V3_AON
GPIO9	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO10	3V3_PEX_RST_MCH#	I	System side PEX reset monitor	10K pull-up to 3V3_AON
GPIO11	ALERT	I/O	Active Low Thermal Alert	100K pull-down
GPIO12	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO13	MEM_VDD	O	GPU Core VDD Power control signal	10K pull-up to 3V3_AON
GPIO14	PWR_LEVEL	I	AC power detect or power ready monitor input	100K pull-up to 3V3_AON
GPIO15	PSI	O	Phase Shedding	10K pull-up to 3V3_AON
GPIO16	HPD_A	O	Hot Plug Detect for HPD used as DisplayPort or for HPD when used as Dual Link DVI	See Figure 12-9
GPIO17	HPD_C	O	Hot Plug Detect for HPD	See Figure 12-9
GPIO18	HPD_B	O	Hot Plug Detect for HPD	See Figure 12-9
GPIO19	HPD_F or HPD_B	O	Hot Plug Detect for HPD or for HPD when used as DisplayPort	See Figure 12-9
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PEX reset control	10K pull-up to 3V3_AON
Pin Name	Normal Function	IO	Functional Description	Recommended Default Pull-up or Pull-down
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON

Table 114. G82-64 and G84-128 GPIO Description

Pin Name	Normal Function	IO	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MCH	I	FB Clamp monitor	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VDD	10K pull-up to 3V3_AON
GPIO2	LC0D_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LC0D_VCC	O	Panel Power Enable	100K pull-down
GPIO4	LC0D_BL_EN	O	Panel Backlight Enable	100K pull-down
GPIO5	Reserved			
GPIO6	FB_CLAMP_TGL_REQ	O	Active Low FB Clamp trigger request	10K pull-up to 3V3_AON
GPIO7	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO8	OVERT	O	Active Low Thermal Catastrophic Over Temperature	100K pull-down
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-down
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VDD	O	GPU Core VDD Power control signal	10K pull-up to 3V3_AON
GPIO12	PWR_LEVEL	I	AC power detect or power ready monitor input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON
GPIO14	HPD_A	O	Hot Plug Detect for HPD used as DisplayPort or for HPD when used as Dual Link DVI	See Figure 12-9
GPIO15	HPD_C	O	Hot Plug Detect for HPD	See Figure 12-9
GPIO16	HPD_B	O	Hot Plug Detect for HPD	See Figure 12-9
GPIO17	HPD_F	O	Hot Plug Detect for HPD or for HPD when used as DisplayPort	See Figure 12-9
GPIO18	Reserved			
GPIO19	Reserved			

• GPIO20 and GPIO21 are only available on H54M-LV/LS/RE/HS H54M-GV/GR/GT  
 • The greyed out section of Table 107 indicates GPIOs that are not available for H54M-G2/-G4

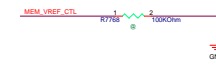
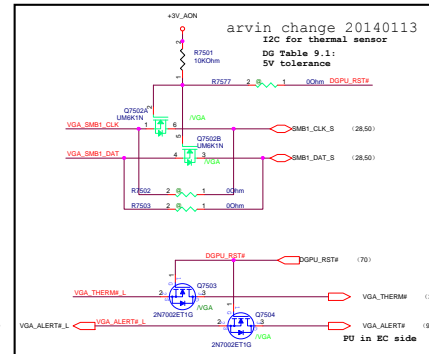
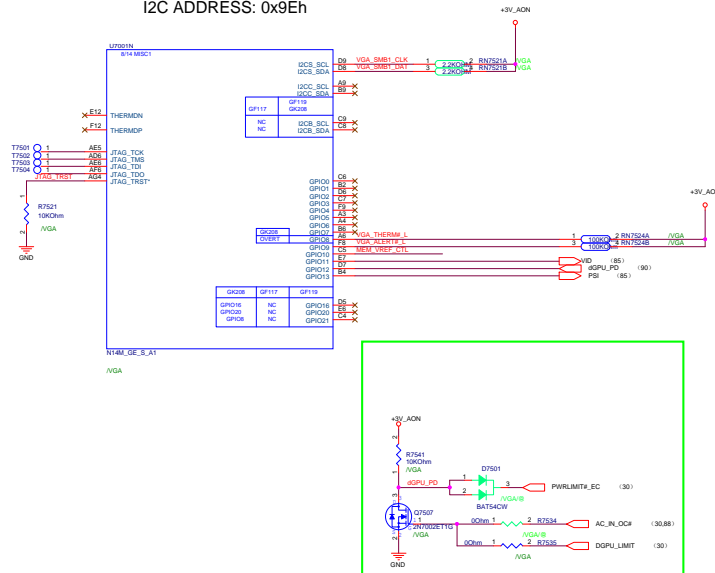
Table 7. GPIO Differences

GPIO Pin	GPU	Normal Function	Comments
GPIO0	H15V-GM	RESERVED	Leave as IIC
	H155-GV	RESERVED	Connect to FB_CLAMP_MCH circuitry.
	H155-GM/-GT	FB_CLAMP_MCH	If H155-GM/-GT are designed into H14x motherboard with GC6 1.0, connect GPIO0 to FB_CLAMP_MCH circuitry. If H155-GM/-GT are designed into H15x motherboard with GC6 2.0, use GPIO0 as the GC6_FB_EH function.
GPIO5	H15V-GM	RESERVED	Leave as IIC
	H155-GV	RESERVED	Leave as IIC
	H155-GM/-GT	RESERVED	If H155-GM/-GT are designed into H14x systems; or 3V3_MAIN_EN in H15x systems as IIC. If H155-GM/-GT are designed into H15x motherboard with GC6 2.0, use GPIO5 as the 3V3_MAIN_EN function.
GPIO6	H15V-GM	RESERVED	Leave as IIC
	H155-GV	FB_CLAMP_TGL_REQ	Connect to FB_CLAMP_TGL_REQ# circuitry.
	H155-GM/-GT	FB_CLAMP_TGL_REQ	If H155-GM/-GT are designed into H14x motherboard with GC6 1.0, connect GPIO6 to FB_CLAMP_TGL_REQ# circuitry. If H155-GM/-GT are designed into H15x motherboard with GC6 2.0, use GPIO6 as the GPU_EVENT# function.

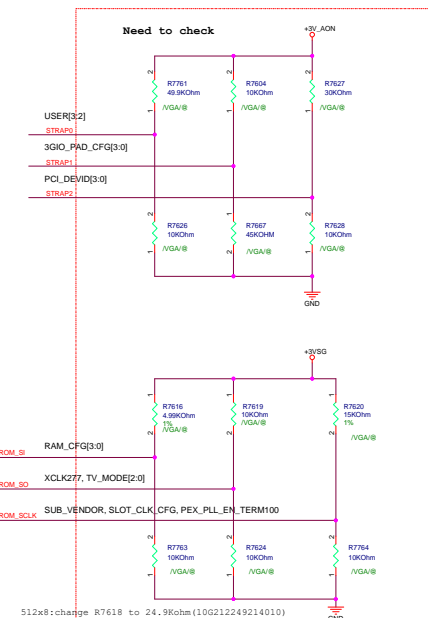
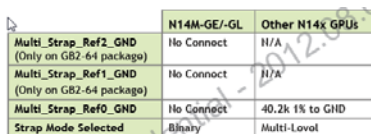
GPIO Pin	GPU	Normal Function	Comments
GPIO8	H15V-GM	OVERT	Connect to OVERT circuitry.
	H155-GV	RESERVED	RESERVED in H14x systems; or SYS_PEX_RST_MCH# in H15x systems
	H155-GM/-GT	RESERVED	The OVERT function is provided on the dedicated OVERT pin on G82B-64, which is on the same pin as GPIO8 on G82-64. GPIO8 on G82B-64 is a system PEX reset monitor function for GC6 2.0. If H155-GM/-GT are designed into H14x motherboard with GC6 1.0, leave GPIO8 as IIC. If H155-GM/-GT are designed into H15x motherboard with GC6 2.0, use GPIO8 as the SYS_PEX_RST_MCH# function.
GPIO14, GPIO15, GPIO17, GPIO18, GPIO19	H15V-GM	N/A	Leave as IIC
	H155-GV	Display HPD	Leave as IIC if HPD function is not required. See H15x Design Guide, DG-06803-001, for which IIP link should be paired with which GPIO pin for its HPD function.
	H155-GM/-GT	Display HPD	Leave as IIC
GPIO16	H15V-GM	N/A	Leave as IIC
	H155-GV	RESERVED	Leave as IIC
	H155-GM/-GT	RESERVED	Leave as IIC
GPIO20	H15V-GM	N/A	Leave as IIC
	H155-GV	RESERVED	Leave as IIC
	H155-GM/-GT	RESERVED	Leave as IIC
GPIO21	H15V-GM	N/A	Leave as IIC
	H155-GV	RESERVED	Leave as IIC
	H155-GM/-GT	RESERVED	If H155-GM/-GT are designed into H14x systems; or GPU_PEX_RST_HOLD# in H15x systems as IIC. If H155-GM/-GT are designed into H15x motherboard with GC6 2.0, use GPIO21 as the GPU_PEX_RST_HOLD# function.

## GPIO, TEMP SENSOR, JTAG

I2C ADDRESS: 0x9Eh



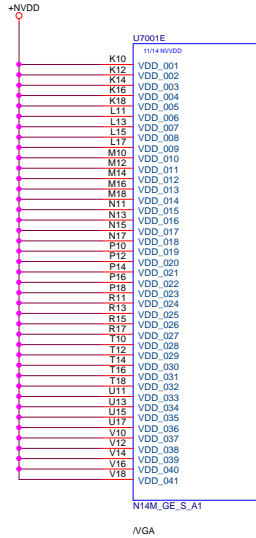
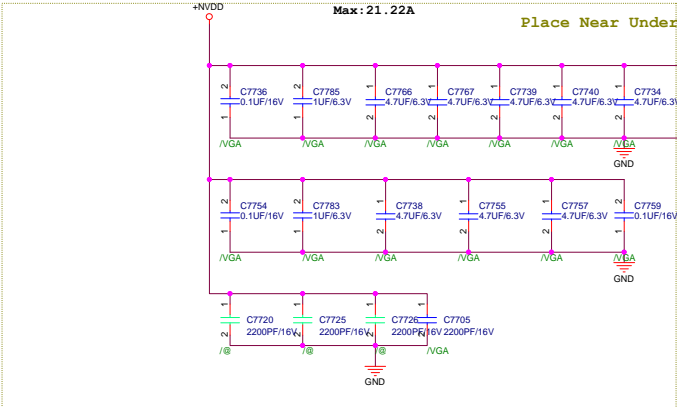
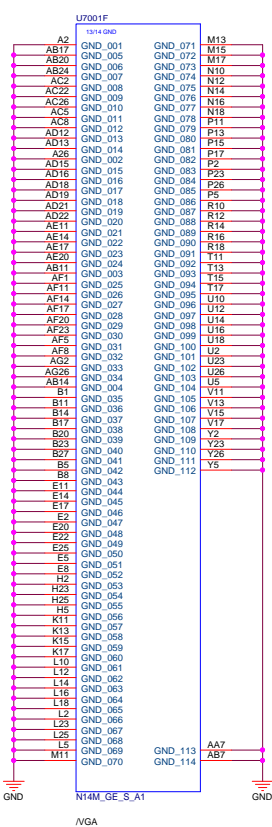


[illegible]

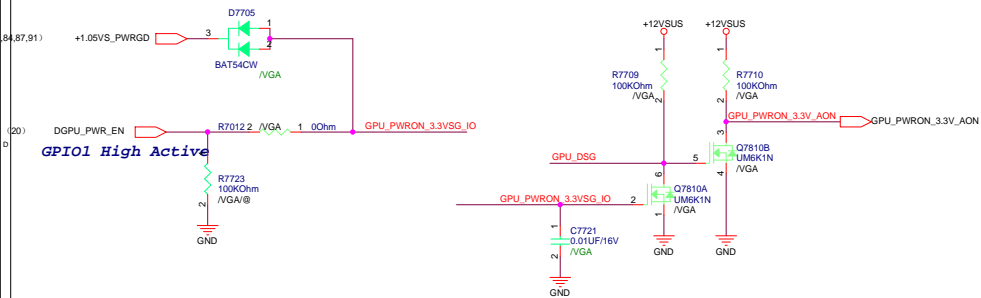
GPU NAME (GPU)		GPU SPECIFICATIONS										
GPU NAME	GPU	VRAM Vendor	Type	FBDVDD / FBDVDDQ	Config	VRAM P/N	Max Speed CLK	I/V Mini	RAM_CFG	ROM_SIZE	Status	
GM108	N155-Q1/OM	Hynix	DDR3	1.5V/7.5V	128Mb16	H5TCJ2G63FF-R-11C	1000MHz	NA	0x6	PD 35K	Prefinitia	
		Microon	DDR3	1.5V/1.5V	128Mb16	MT41L128M16T1-093G-K	1000MHz	1322	0x7	PD 45K	Prefinitia	
		Samsung	DDR3	1.5V/1.5V	128Mb16	K4W201646G-BC1A	1000MHz	NA	0x8	PU 5K	Prefinitia	
		Hynix	DDR3	1.5V/7.5V	256Mb16	H5TC4063AF-R-11C	1000MHz	NA	0x0	PD 5K	Prefinitia	
		Microon	DDR3	1.5V/7.5V	256Mb16	MT41L256M16HA-093G-E	1000MHz	1322	0x1	PD 10K	Prefinitia	
		Samsung	DDR3	1.5V/7.5V	256Mb16	K4W4G1646G-HC1A	1000MHz	NA	0x2	PD 15K	Prefinitia	
		Hynix	DDR3L	1.35V / 1.35V	128Mb16	H5TCJ2G63FF-R-11C	900MHz	NA	0x9	PU 10K	Prefinitia	
		Microon	DDR3	1.35V / 1.35V	128Mb16	MT41L128M16T1-093G-K	900MHz	1322	0x4	PU 15K	Prefinitia	
		Samsung	DDR3L	1.35V / 1.35V	128Mb16	K4W201646G-BC1A	900MHz	NA	0x8	PU 20K	Prefinitia	
		Hynix	DDR3L	1.35V / 1.35V	256Mb16	H5TC4063AF-R-11C	900MHz	NA	0x3	PD 20K	Prefinitia	
		Microon	DDR3L	1.35V / 1.35V	256Mb16	MT41L256M16HA-093G-E	900MHz	1322	0x4	PD 25K	Prefinitia	
		Samsung	DDR3L	1.35V / 1.35V	256Mb16	K4W4G1646G-HC1A	900MHz	NA	0x5	PD 30K	Prefinitia	
		Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data	Real Time Clock Data
		Hynix	DDR3	1.5V/1.5V	256Mb16	H5TC4063AF-R-11C	1000MHz	NA	0x0	PD 5K	Prefinitia	
		Microon	DDR3	1.5V/1.5V	256Mb16	MT41L256M16HA-093G-E	1000MHz	1322	0x1	PD 10K	Prefinitia	
		Samsung	DDR3	1.5V/7.5V	256Mb16	K4W4G1646G-HC1A	1000MHz	NA	0x2	PD 15K	Prefinitia	
		Hynix	DDR3L	1.35V / 1.35V	256Mb16	H5TC4063AF-R-11C	900MHz	NA	0x3	PD 20K	Prefinitia	
		Microon	DDR3L	1.35V / 1.35V	256Mb16	MT41L256M16HA-093G-E	900MHz	1322	0x4	PD 25K	Prefinitia	
		Samsung	DDR3L	1.35V / 1.35V	256Mb16	K4W4G1646G-HC1A	900MHz	NA	0x5	PD 30K	Prefinitia	

NVVDD GROUND

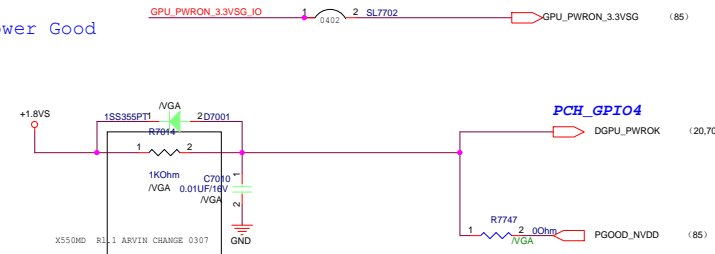
NVVDD POWER AND DECOUPLING



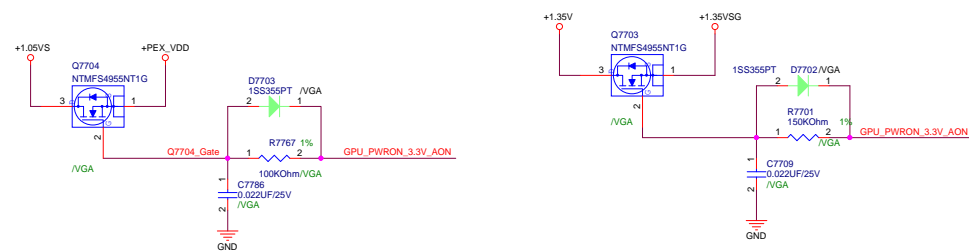
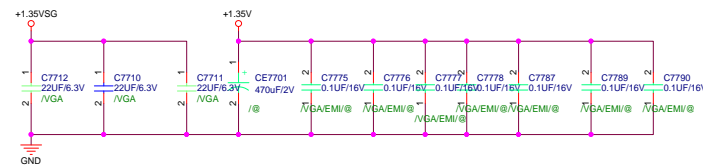
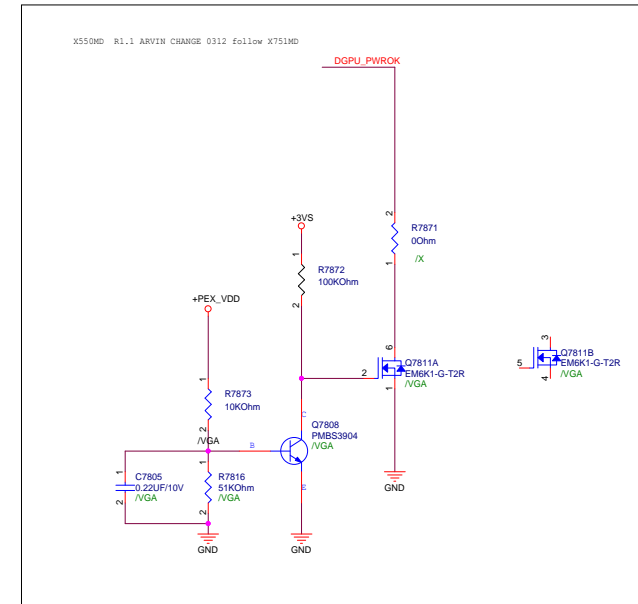
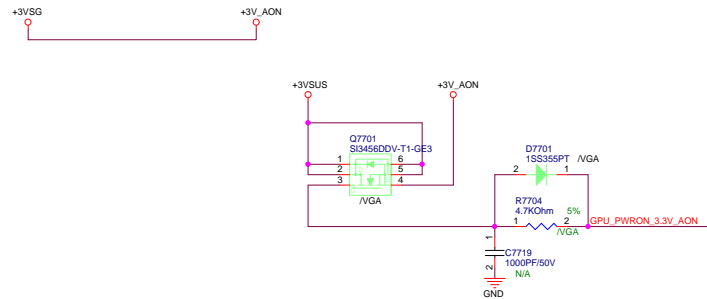
## GPU IO Power Enable



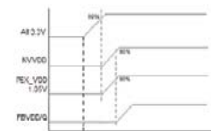
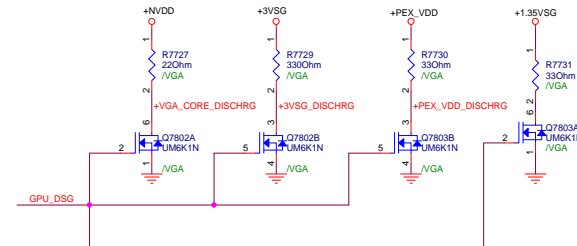
## GPU Power Good



## GPU IO Power



## DSG

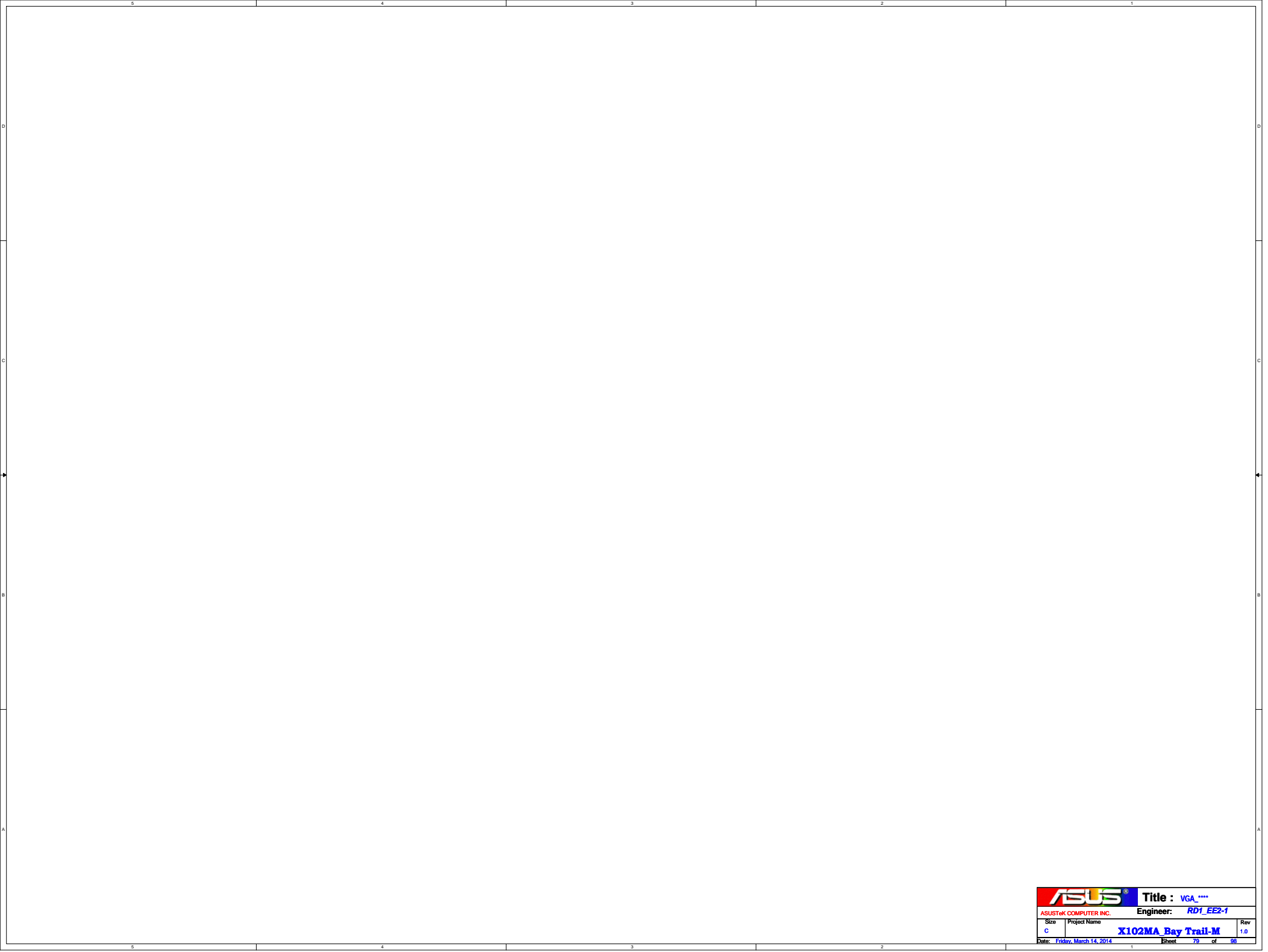


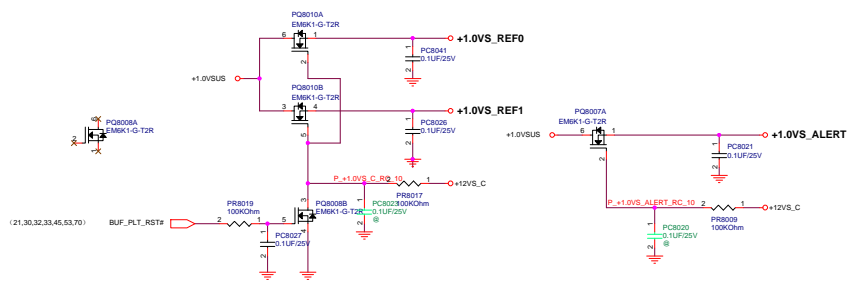
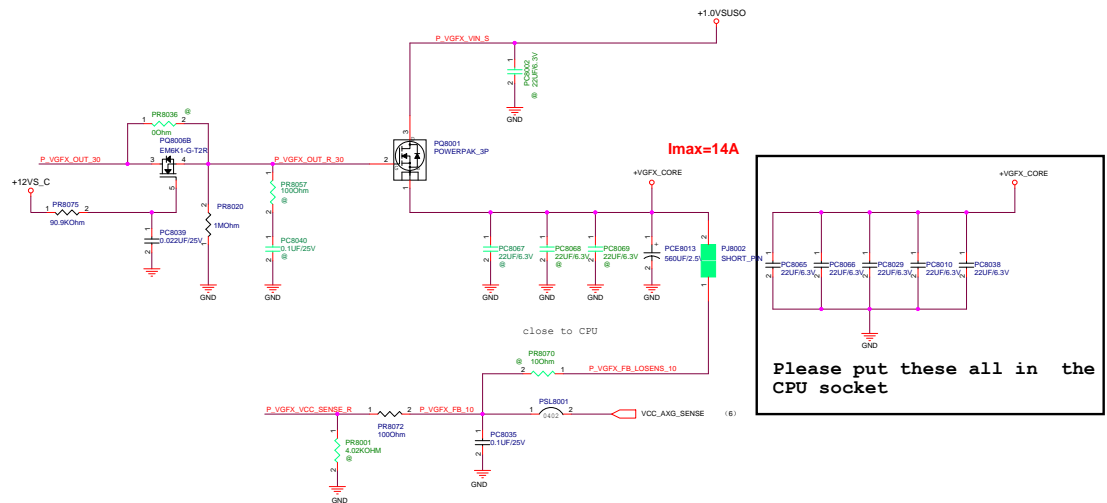
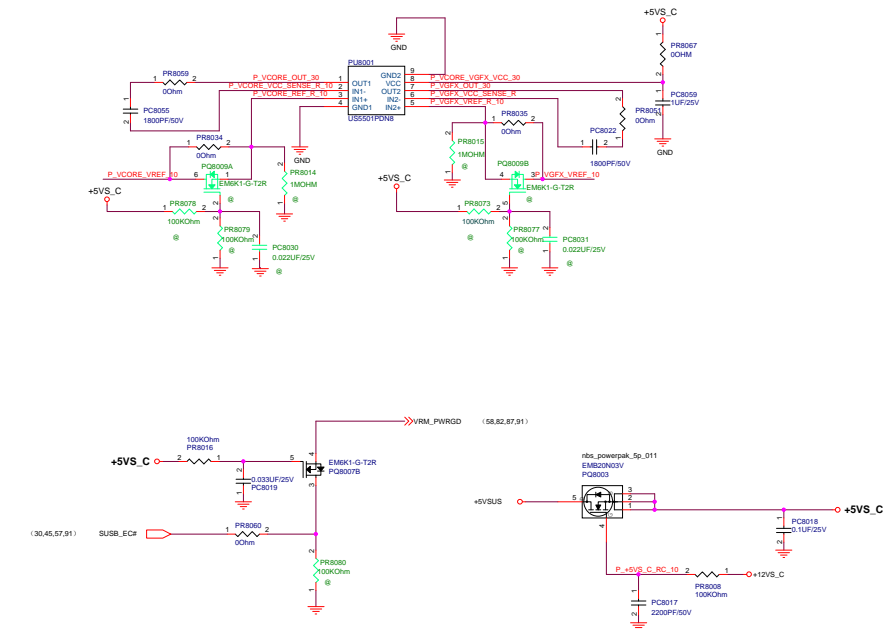
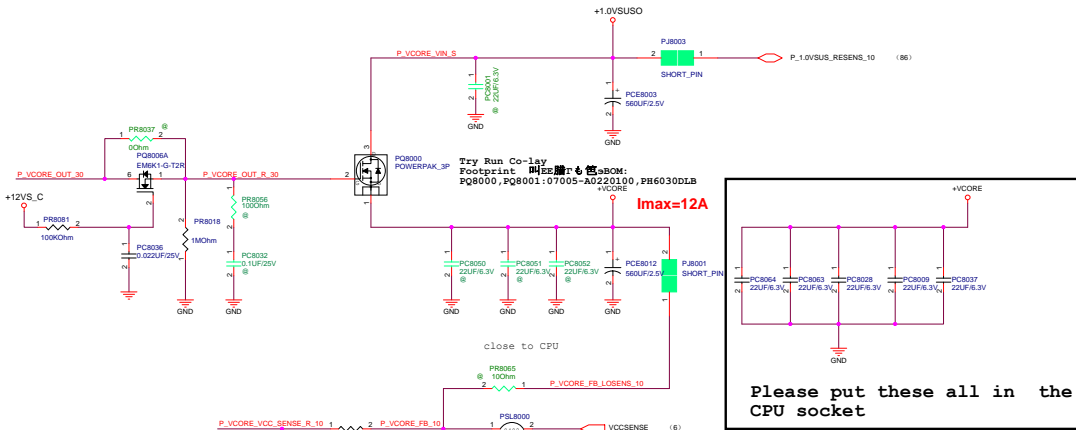
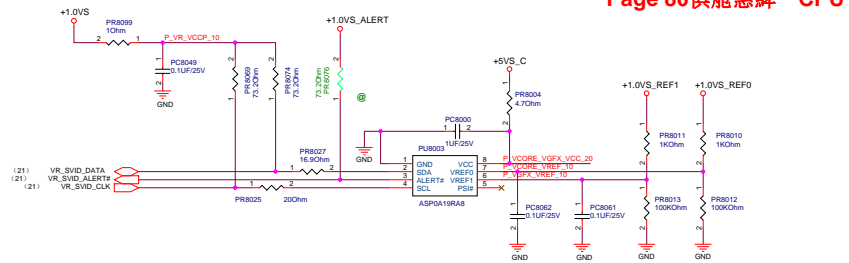
Notes: - All 3.3V includes all rails powered at 3.3V  
- PEX\_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

- Note:
- The ramp time for any rail must be more than 40  $\mu$ s and is recommended to be less than 2ms.
  - The ramp up overshoot should not exceed the silicon reliability limit voltage.
  - A VDD33 must ramp up to 90% before NVDD and PEXVDD in sequence can start ramping up. NVDD must ramp up to 90% before PEXVDD/Q in sequence can start ramping up.
  - No signal should be applied to the GPU before the power rails are fully ramped.
  - Refer to the JEDEC Memory Specification for memory related power sequencing.

<Variant Name>

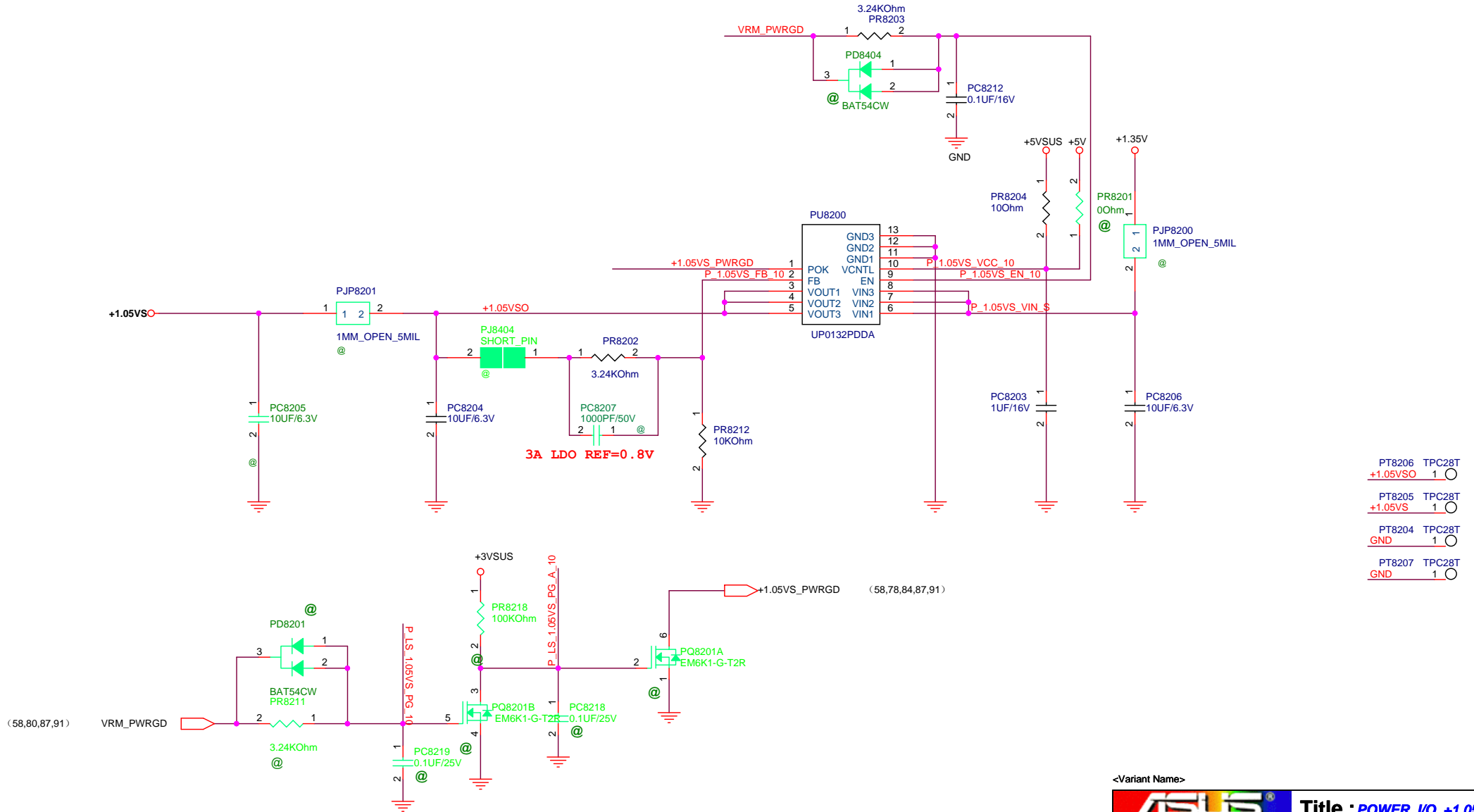




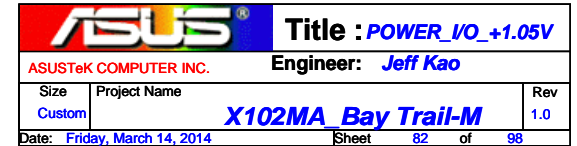
**SUS\_PWRGD**  **SUS\_PWRGD** (21,30,58,86)

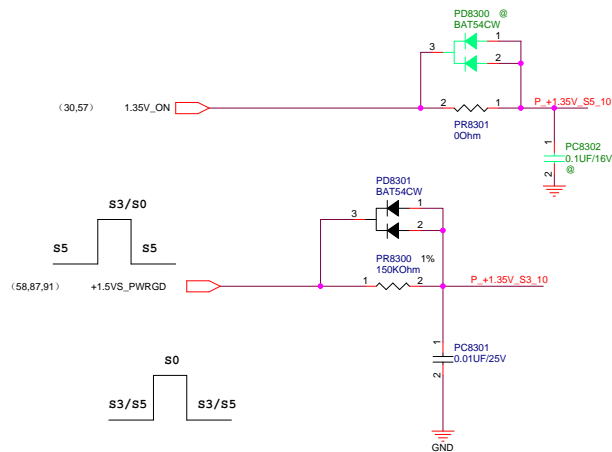


## +1.05VS POWER SUPPLY



<Variant Name>

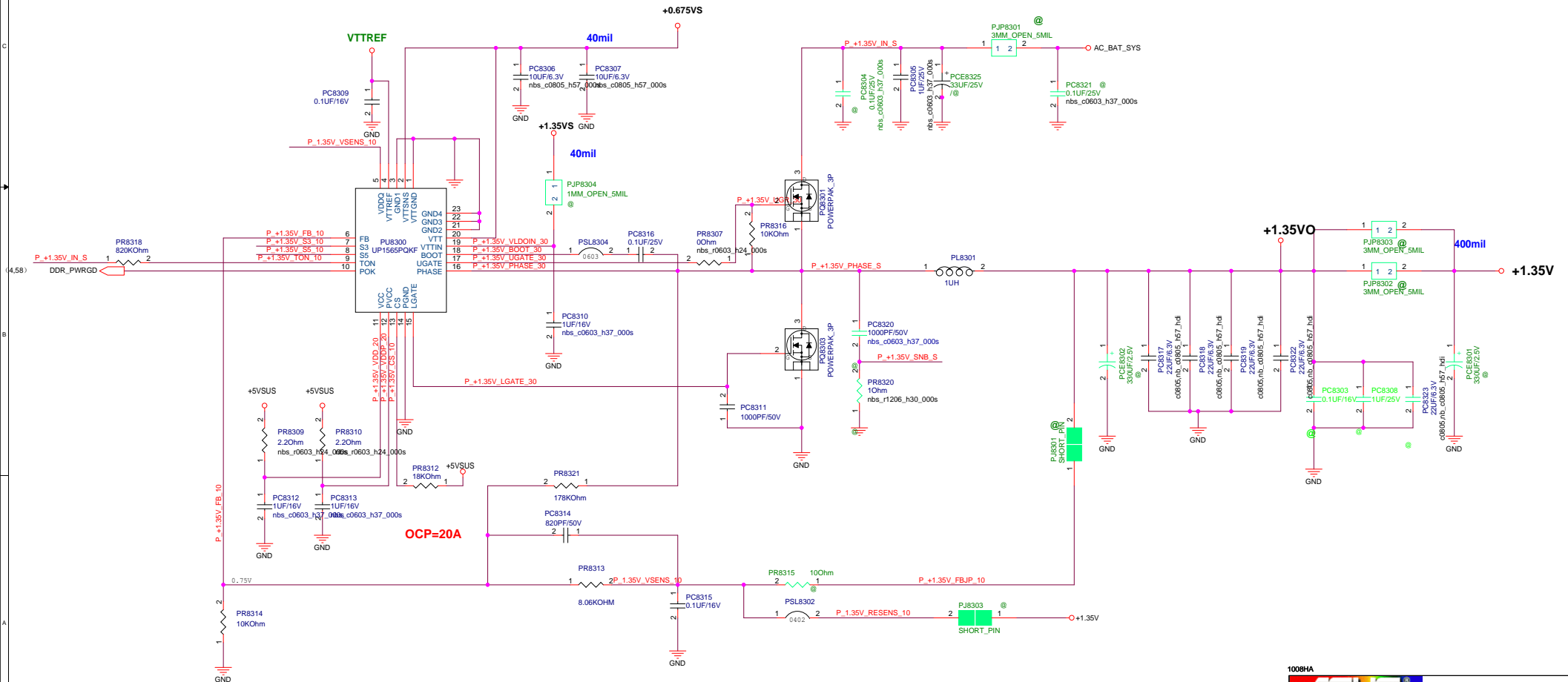




S3 And S5 Truth Table

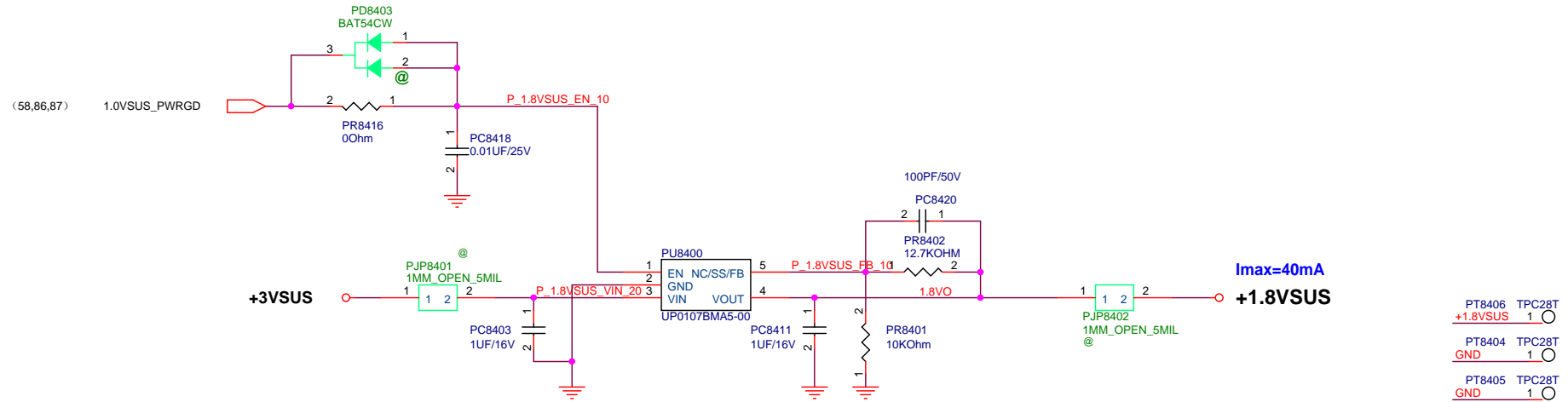
State	S3	S5	VDDQ
S0	Hi	Hi	On
S3	Low	Hi	On
S4/S5	Low	Low	Off (Discharge)

State	VTTREF	VTT
S0	On	On
S3	On	Off(Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)

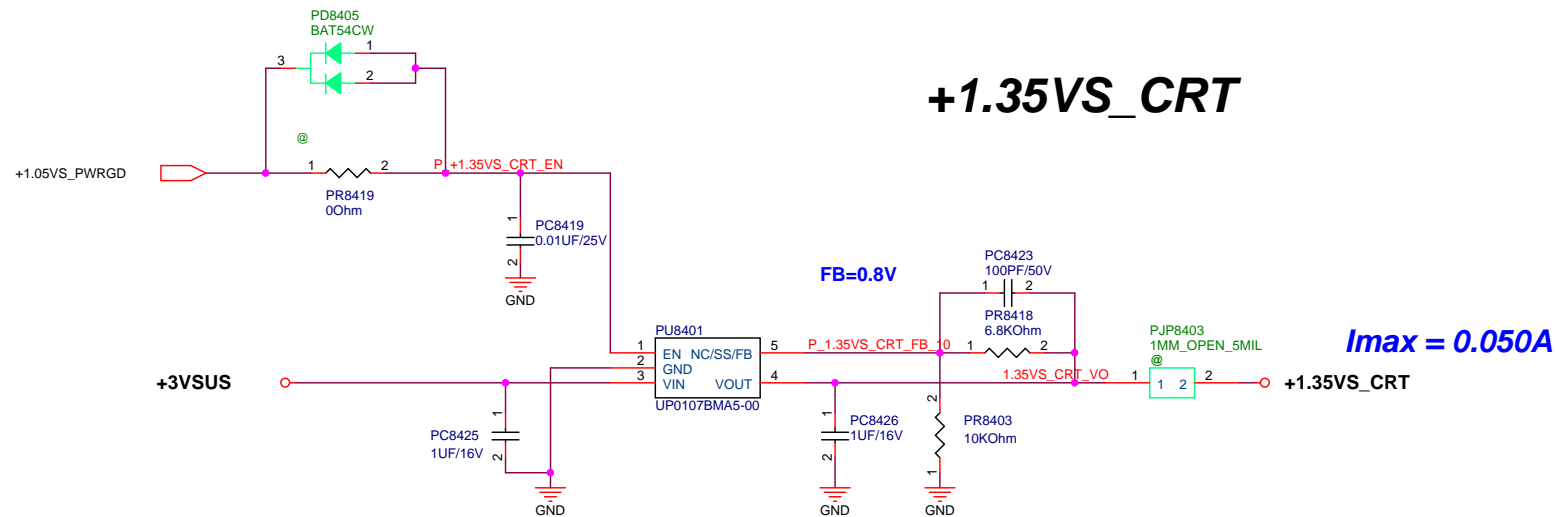




## +1.8VSUS POWER SUPPLY

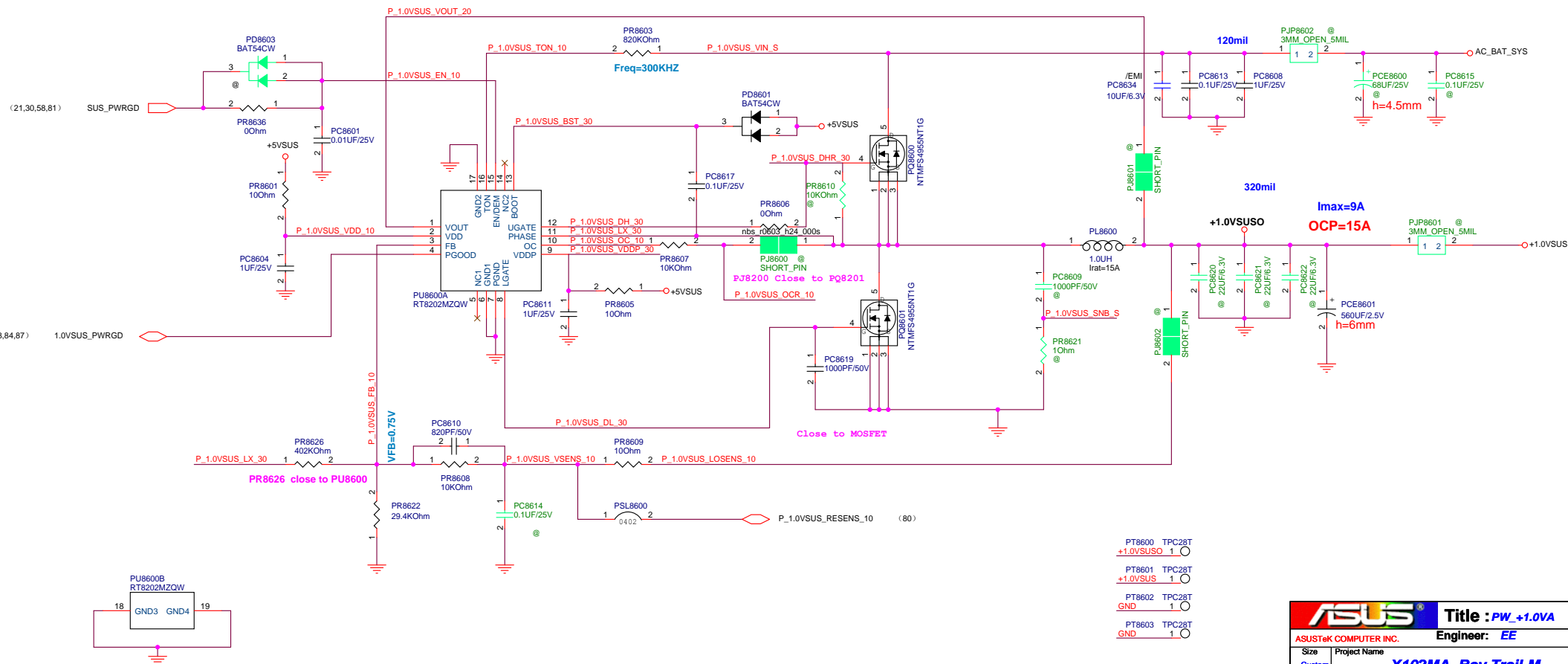



10.8



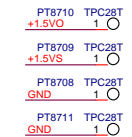
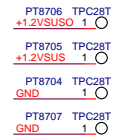


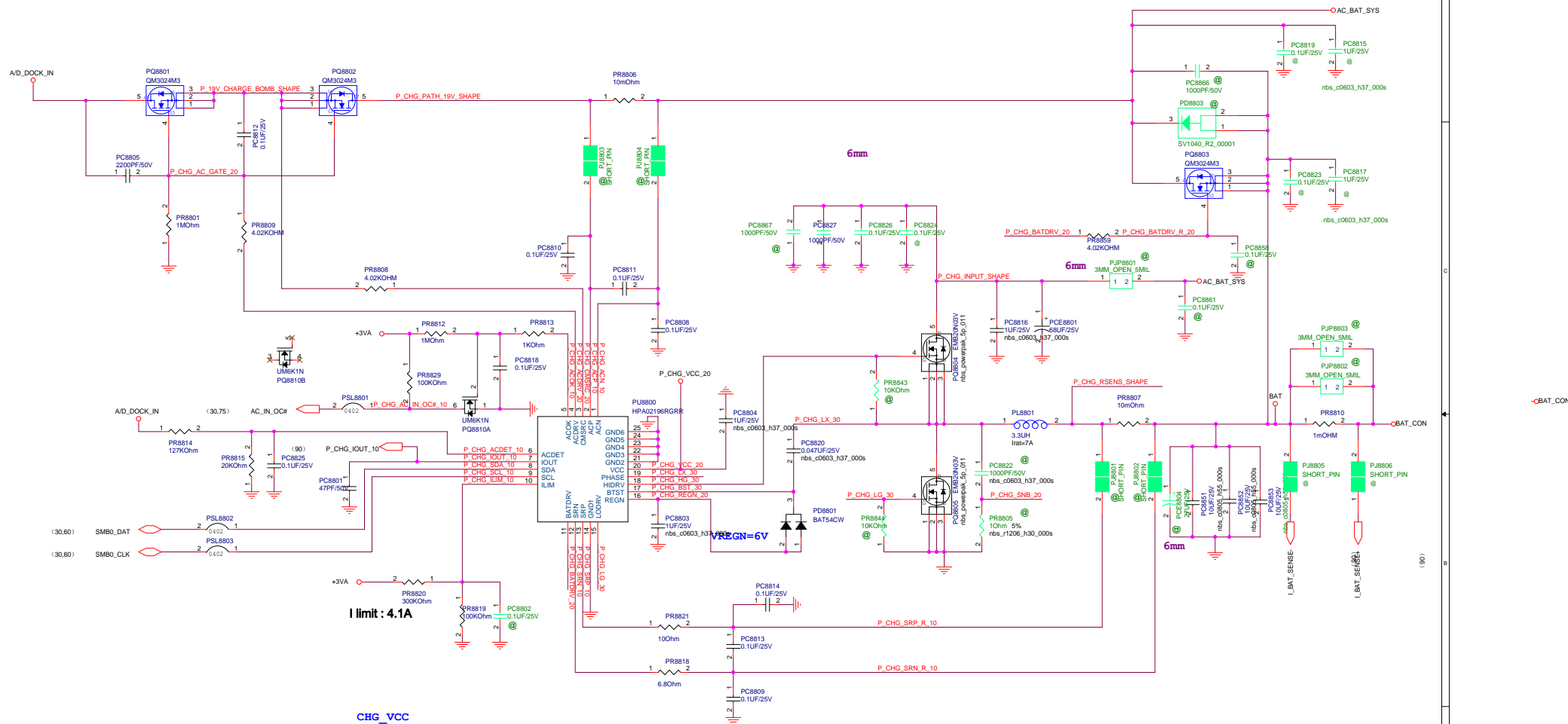
## +1.0VSUS POWER SUPPLY



		<b>Title :</b> <i>PW+1.0VA</i>	
<b>ASUSTek COMPUTER INC.</b>		<b>Engineer:</b> <i>EE</i>	
<b>Size</b> <i>Custom</i>	<b>Project Name</b> <i>X102MA_Bay Trail-M</i>	<b>Rev</b> <i>1.0</i>	
<b>Date:</b> <i>Friday, March 14, 2014</i>	<b>Sheet</b>	<i>86</i>	<b>of</b> <i>98</i>

**+1.5VS**





I limit : 4.1A

CHG\_VCC

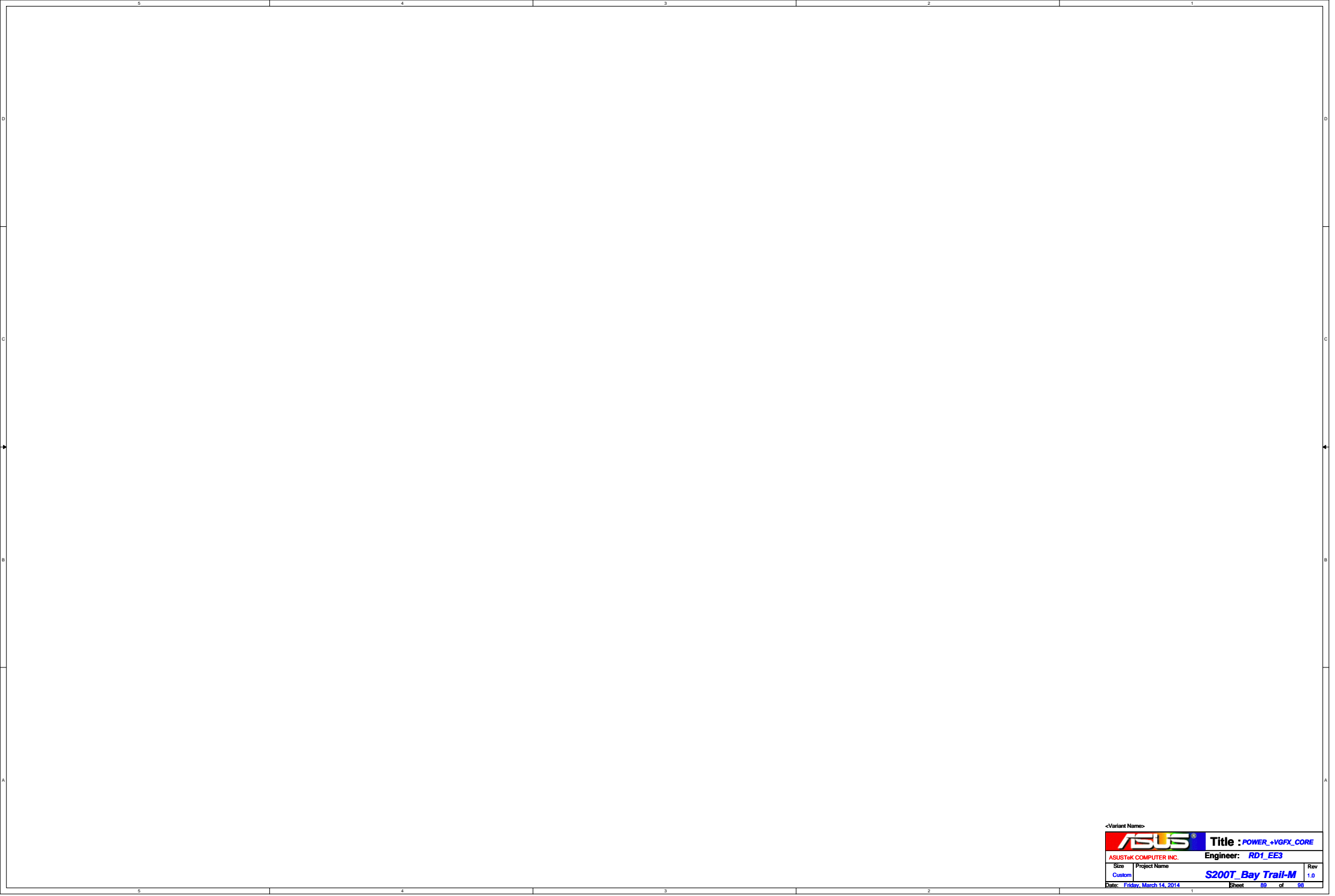
**PR8828 SET**  
 30W : 0.4V =>14k  
 40W : 0.8V =>31.6k  
 45W : 1.2V =>56k  
 65W : 1.6V =>93.1k  
 75W : 2.0V =>150k  
 90W : 2.4V =>270k  
 12W : 2.8V =>56k  
 3.3V =>0

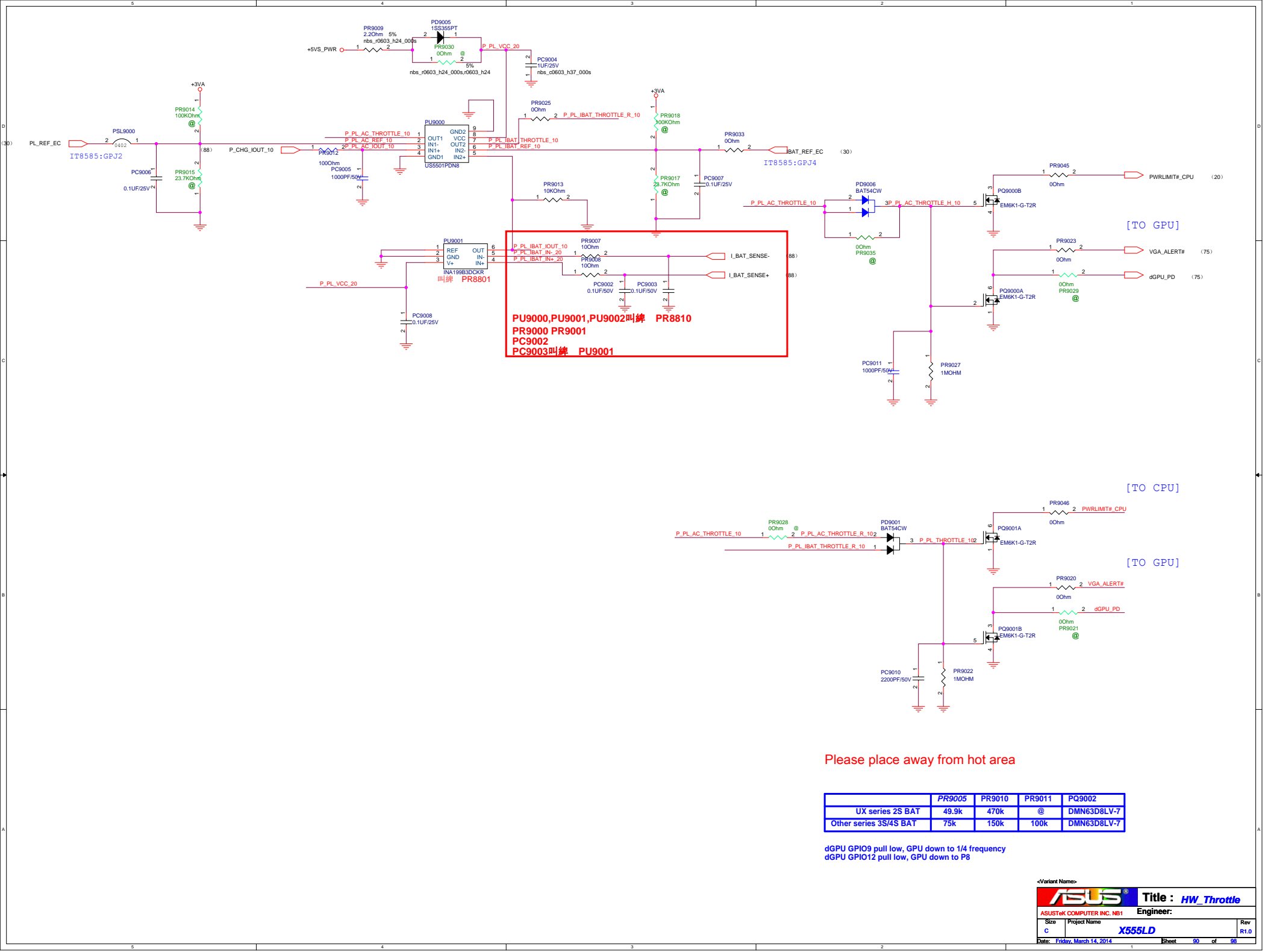
**PR8823, PR8822 SET**  
 PR8823=0 ohm , PR8822 =0 : 4 pin A/D  
 PR8823=0 , PR8822=100Kohm : 4 pin A/D

**PR8822 & PR8823 ; PR8816 & PR8828**  
 Close to U3001 (EC)

**please check page 30,  
 there is no resistors connect to GPI7,GPIO6 pin**

2012\_12\_21



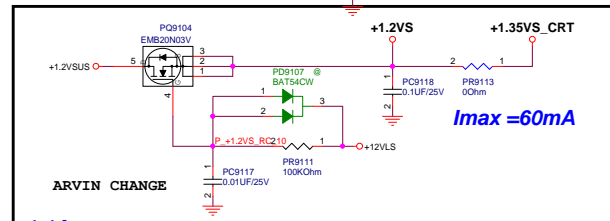
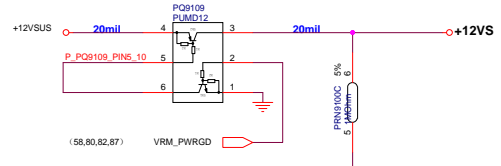
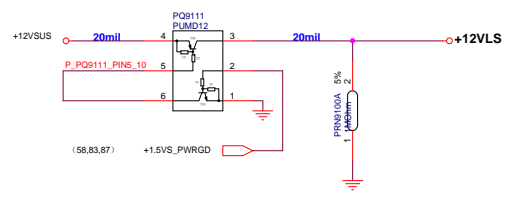
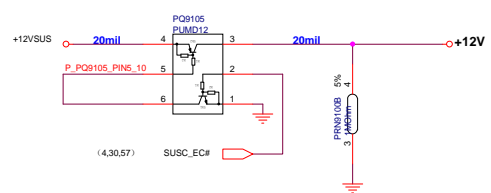
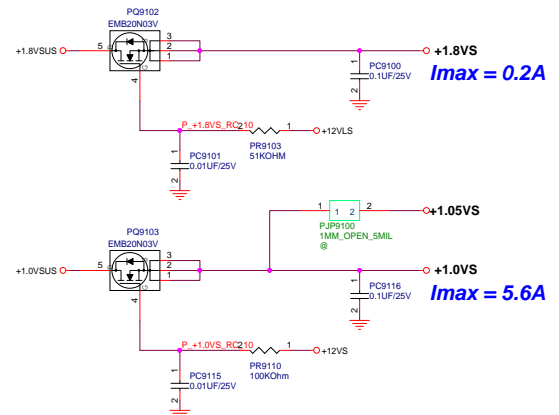
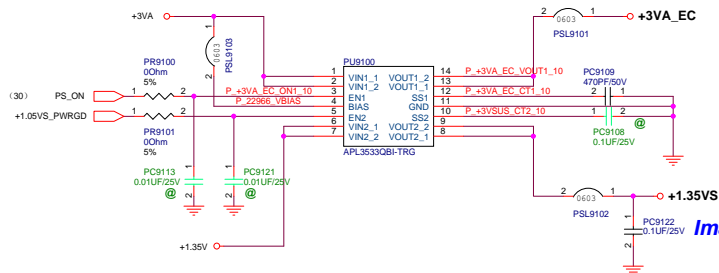
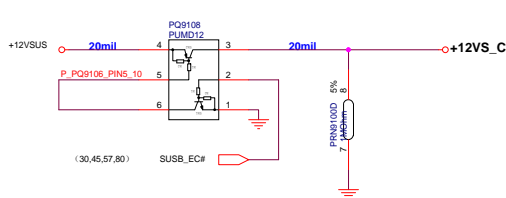
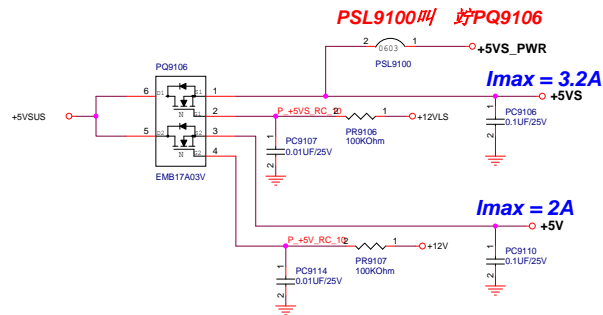
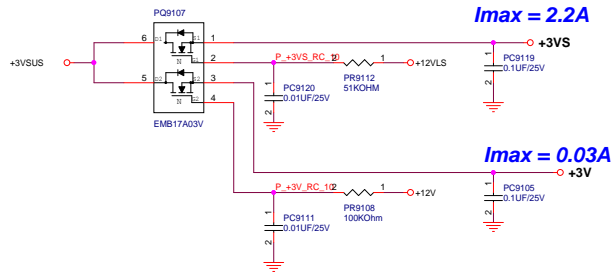


Please place away from hot area

	PR9005	PR9010	PR9011	PQ9002
UX series 2S BAT	49.9k	470k	@	DMN63D8LV-7
Other series 3S/4S BAT	75k	150k	100k	DMN63D8LV-7

dGPU GPIO9 pull low, GPU down to 1/4 frequency  
dGPU GPIO12 pull low, GPU down to P8

# Load Switch



<Variant Name>

<b>ASUS</b>		<b>Title : Load Switch</b>	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size	Project Name	X102MA Bay Trail-M	
Custom		Rev 1.0	
Date: Friday, March 14, 2014	Sheet	81	of 98









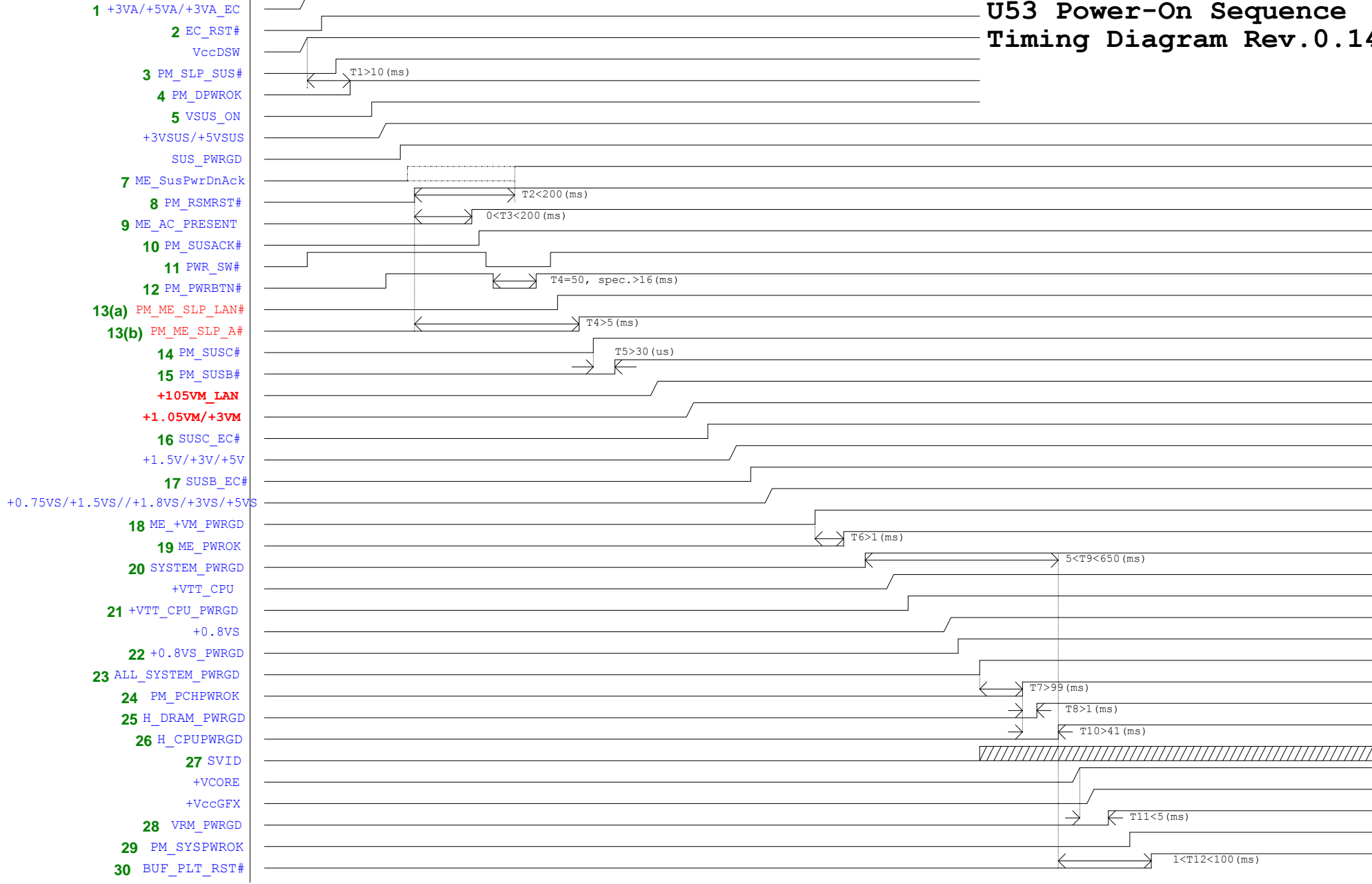
[illegible]

## U53 Power On Sequence Diagram Rev.0.14



AC-IN Mode

U53 Power-On Sequence  
Timing Diagram Rev.0.14



DC-IN Mode

U53 Power-On Sequence  
Timing Diagram Rev.0.14

